

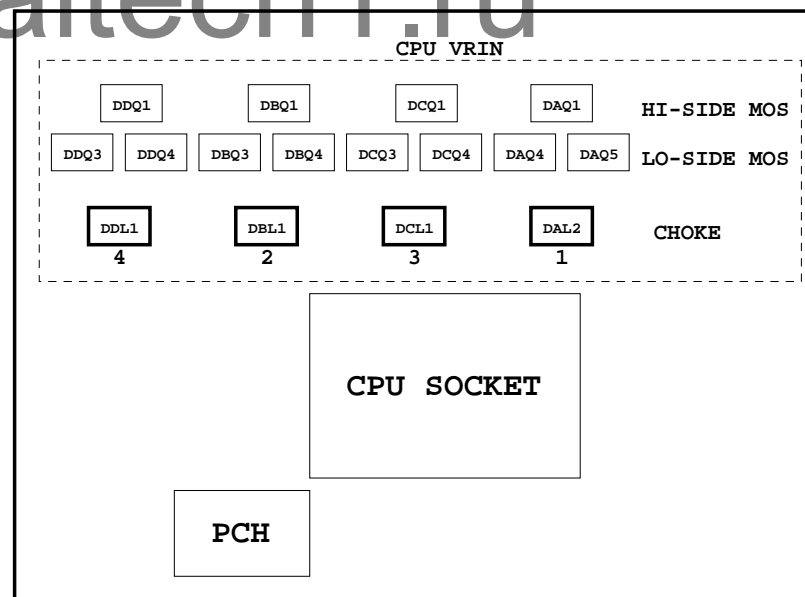
Model Name: GA-B85-D3V-SI 2.01

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_RGB,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCIEX1*2 , PCIEX4 SLOT
16	ITE8892 PCI BRIDGE
17	PCI SLOT 1&2
18	I/O ITE8728
19	COM, -PROHOT, R_USB
20	Dual BIOS / LPT
21	ALC892 CODEC
22	REAR AUDIO JACK
23	VCORE_ ISL95820_1
24	VCORE_ ISL95820_2
25	DDR15V / M3 POWER
26	NCP3933 OVER VOLTAGE
27	DISCRETE POWER

SHEET TITLE

28	F_PANEL , F_USB2.0/3.0
29	ATX POWER, CLOCK GEN
30	HWM , KB/MS , FAN CTRL
31	Realtek RTL8111G
32	DVI
33	HDMI
34	TABLE LIST
35	
36	
37	
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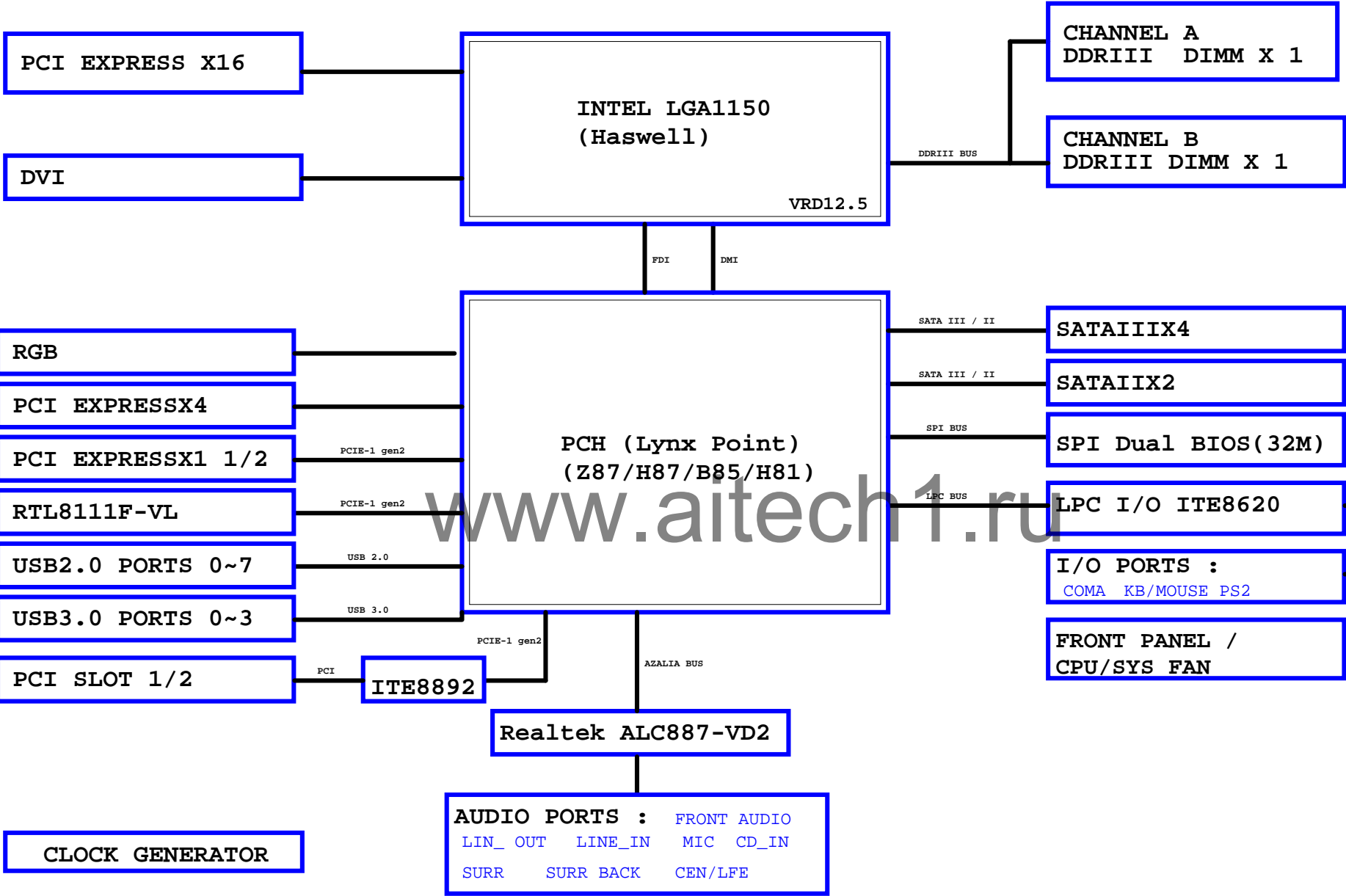


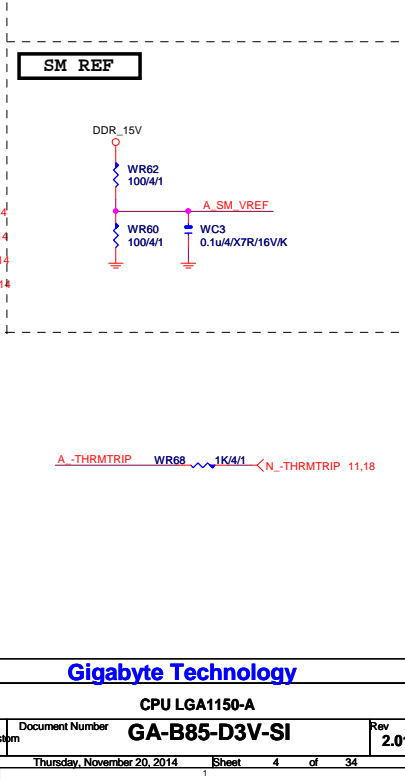
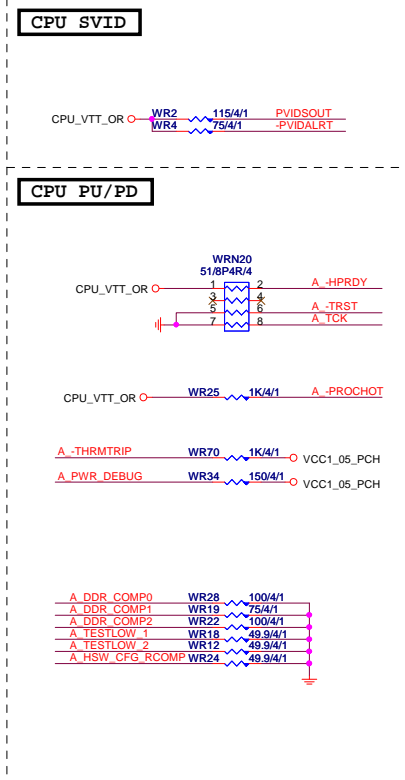
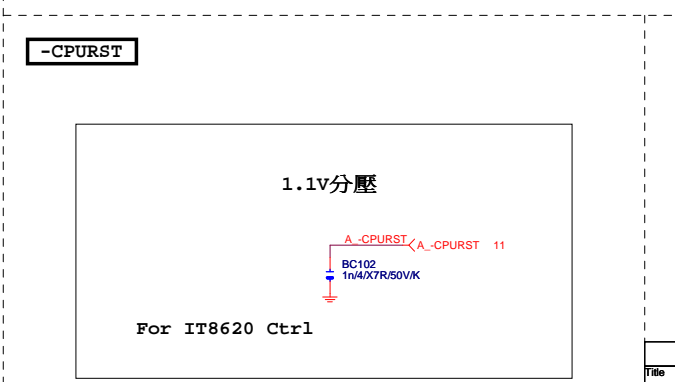
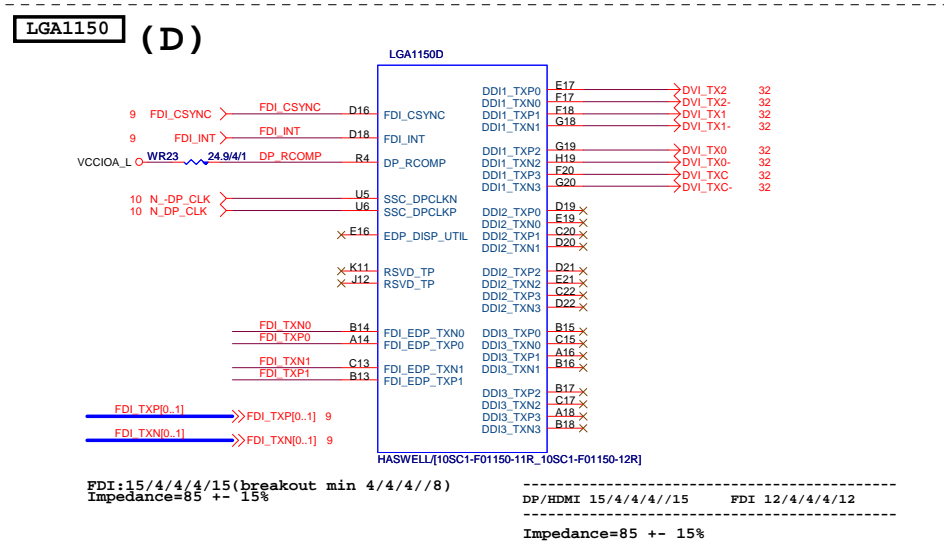
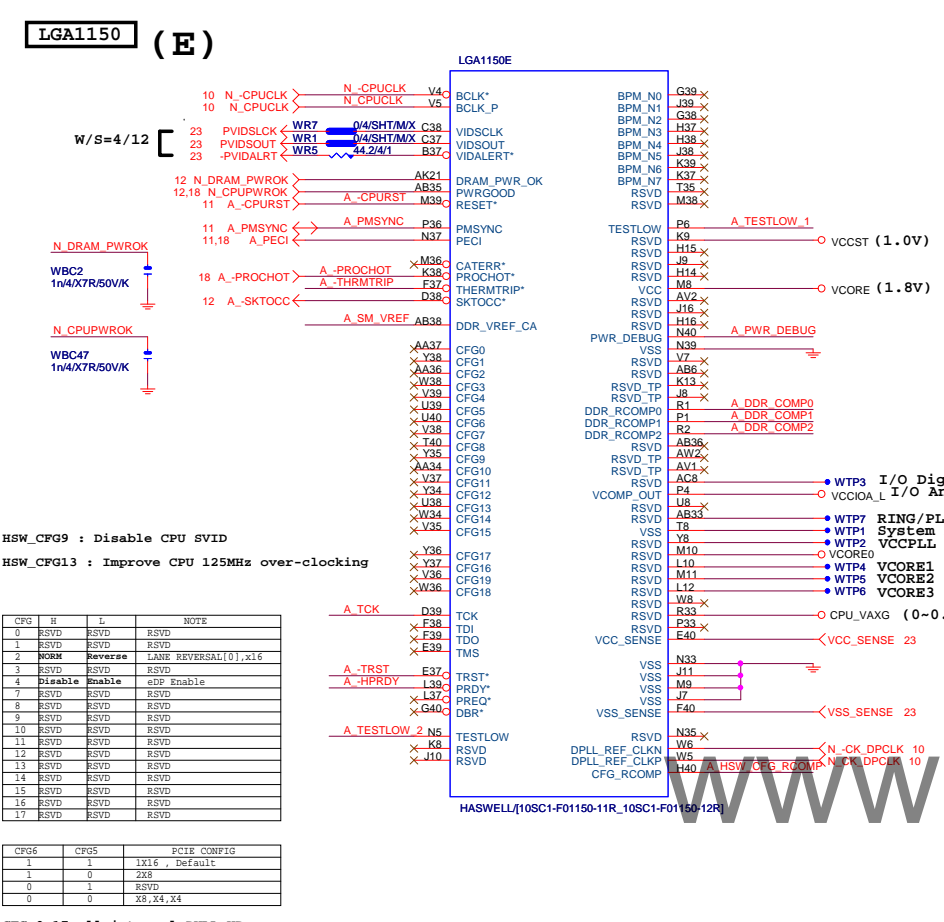
## Component value change history

[illegible]

DATE	Change Item	Reason
0.1	1. H81-HD3 Rev1.02 --> B85-D3V Rev0.1	
0.2	1. IT8892右上角的VCC3切割加大 2. VCC和+12切割加大 3. F_USB ESD change to "3VDUAL" + OP 4. 0ohm --> short pad	
0.3		
1.1	1. Update "POLYSWITCH-1206-1" 2. 所有的PPAK footprint改為Q_TDS08-GDS-T (增加NXP相容) 3. PE_SRCCLK_3GIO1/PE_-SRCCLK_3GIO1 change to PCH pin W6/W7	
2014/05/12 PCB:2.0	1. LAN to RTL8111G 2. VCORE MOSFET to 1上1下 3. H81 series Cost down rule 4. K/B_MOUSE排阻0402改為0603 5. DVI remove level shift 6. Remove 短路保護 7. 1206 3.5A fuse to 0805 2.6A 8. Remove 3933	
2014/06/20 PCB:2.01	1.SATA / SATA Express remove MLCC,3.修改為short pad + Mask ; PCB跳小版本(次版次)	
2014/11/19 PCB:2.01	1.RENAME B85-D3V-SI FOR SI客戶	

BLOCK DIAGRAM





**(A)**

LGA1150A

HASWELL/[10SC1-F01150-11R\_10SC1-F01150-12R]

(B)

LGA1150B

HASWELL/10SC1-F01150-11R\_10SC1-F01150-12R

(CR)

## DDR BUS

7 MODT\_A[0..1]  $\longleftrightarrow$  MODT\_A[0..1]  
8 MODT\_B[0..1]  $\longleftrightarrow$  MODT\_B[0..1]

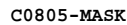
**(F, J)**



**(G,H,I)**



(x18)



( x9 )



## Gigabyte Technology

Title			
CPU LGA1150-C			
Size	Document Number		Rev
Custom	GA-B85-D3V-SI		2.01
Date:	Thursday, November 20, 2014	Sheet	6 of 34

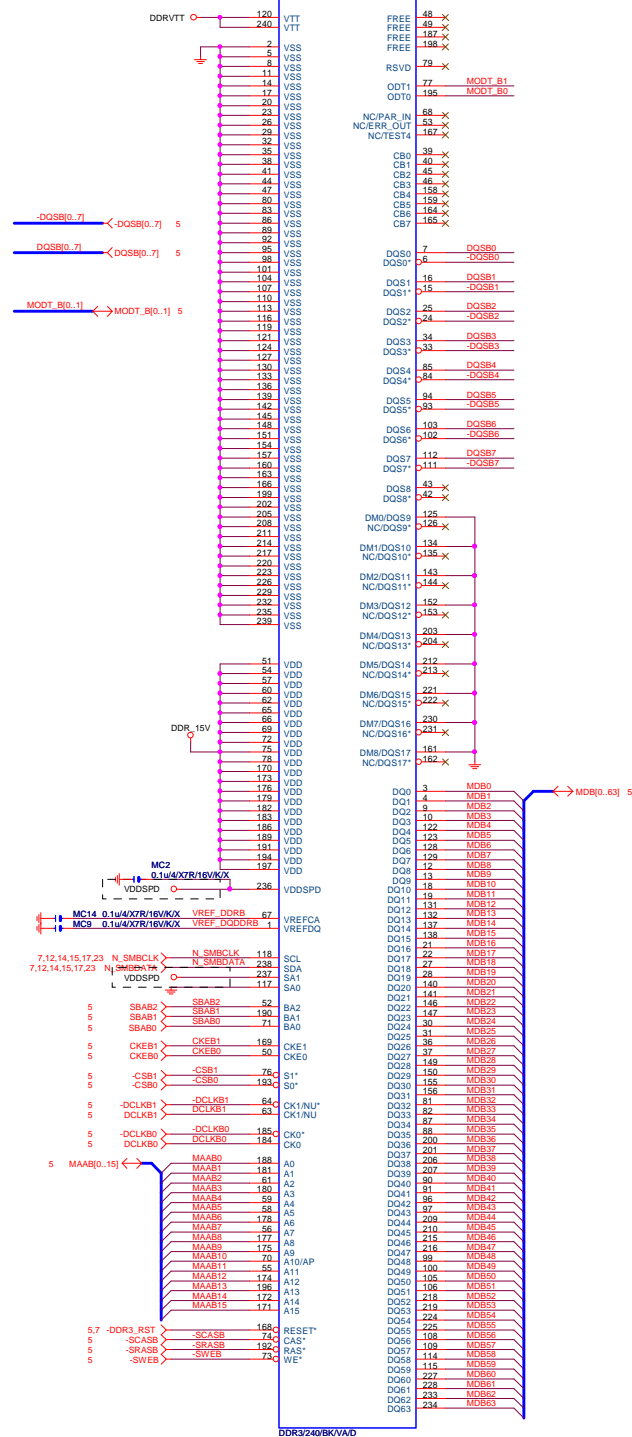




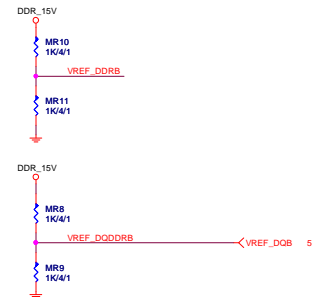
DDR3

(B)

DDR3\_2



DDR3 VREF



DDR3 1066,1333,1600MHZ BANDWIDTH

DDR3 1066MHZ  
DDR3 clock=533MHZ  
DDR3 single channel bandwidth=533x2x8Byte=8.5GB/s  
DDR3 dual channel bandwidth=533x2x2x8Byte=17GB/s

DDR3 1333MHZ  
DDR3 clock=667MHZ  
DDR3 single channel bandwidth=10.6GB/s  
DDR3 dual channel bandwidth=21GB/s

DDR3 1600MHZ  
DDR3 clock=800MHZ  
DDR3 single channel bandwidth=12.8GB/s  
DDR3 dual channel bandwidth=25.6GB/s

COUPON



CPU

DIMM1 (黑色) CHA

DIMM2 (黑色) CHB

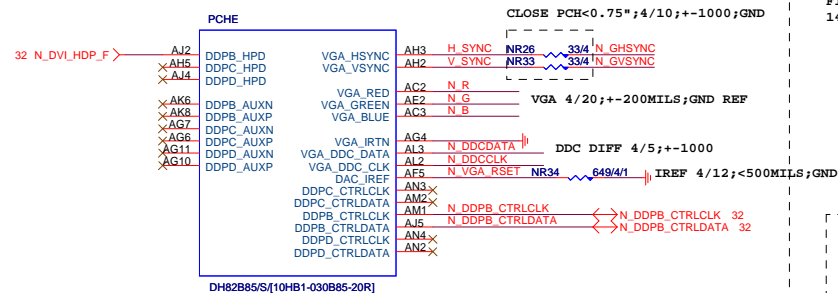
Gigabyte Technology

File	DDR3 CHANNEL B	Rev	2.01
Size	Document Number	GA-B85-D3V-SI	
Custom			
Date:	Sheet	8	of 34





# PCH (E)

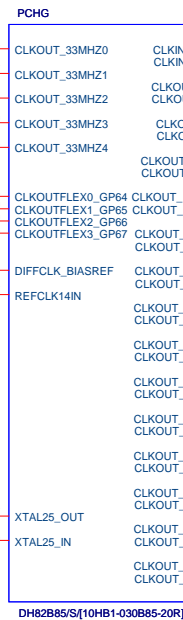
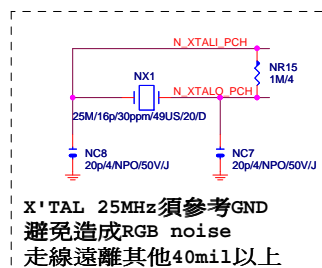


VGA DISABLE
R,G,B NC OR GND
IRTN / IREF GND
VGA_HSYNC, VGA_VSYNC, DDC_CLK, DDC_DATA NC
POWER VCCADAC(AF2), VCCADACBG(AE1) GND

# PCH (G)

Flex1,2,3,4 :  
 14/24/33/48MHZ

VCC1\_5\_PCH  
 [9] N\_PCHCLK14

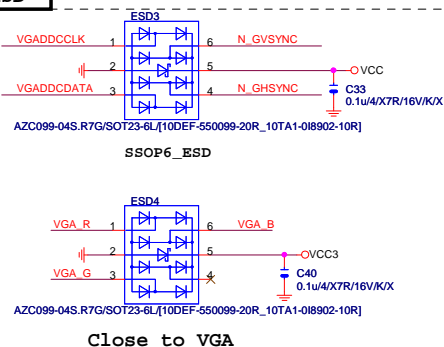


Differential Clock: 18/4/6/4/18  
 Impedance=90 +- 15%

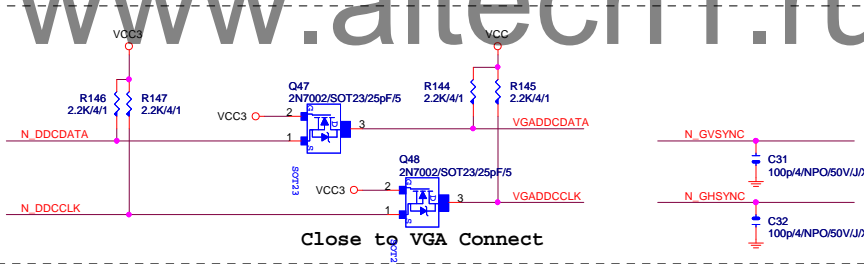
# PCH CLK PD



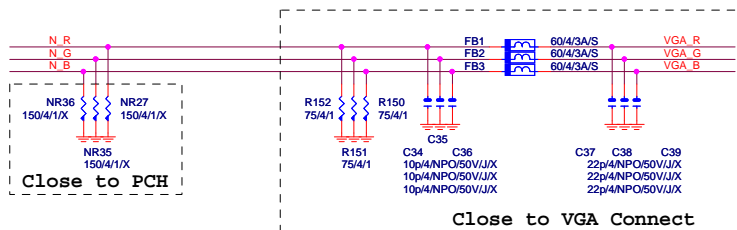
# VGA ESD



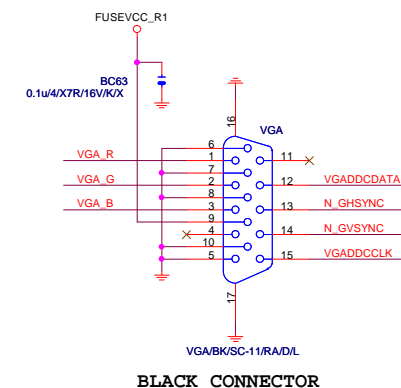
# VGA DDC



# VGA DDC



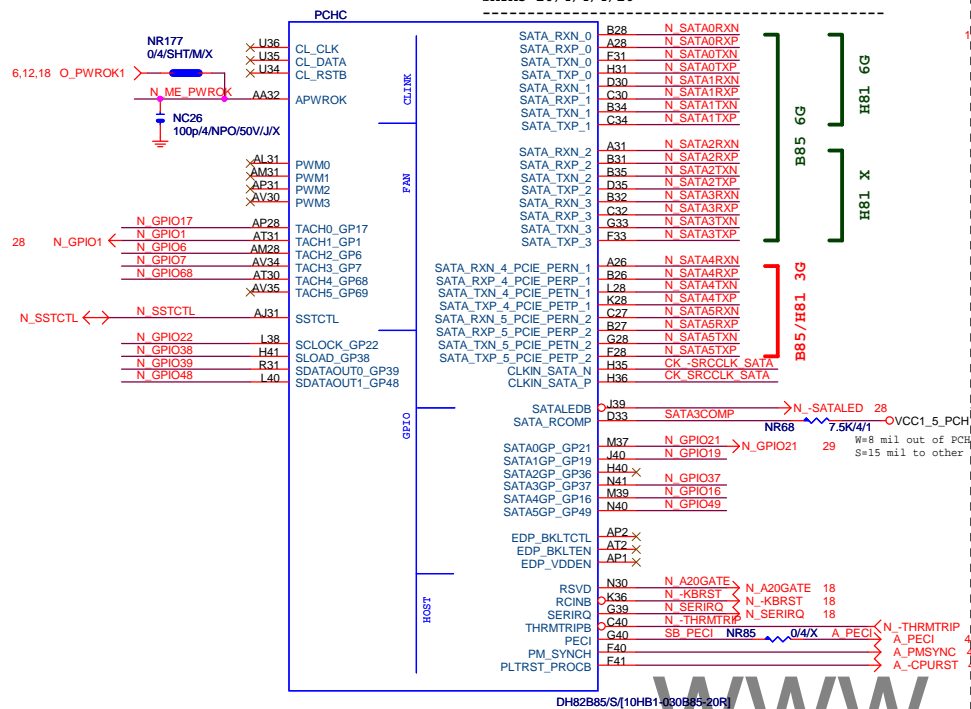
# VGA CONNECTOR



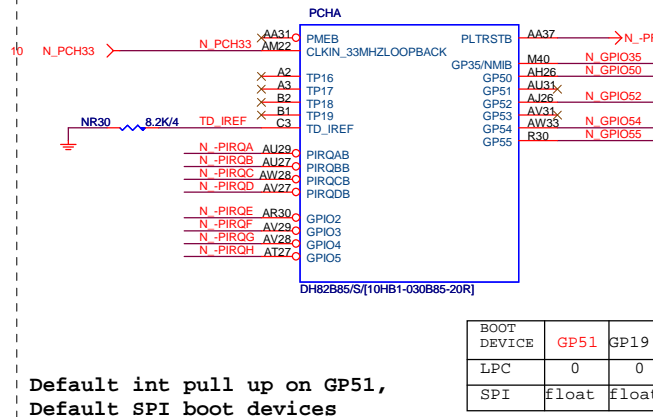
# Gigabyte Technology

Title	PCH DISPLAY ,CLK BUFFER		
Size	Document Number	Rev	2.01
Customer	GA-B85-D3V-SI		
Date	Thursday, November 20, 2014	Sheet	10 of 34

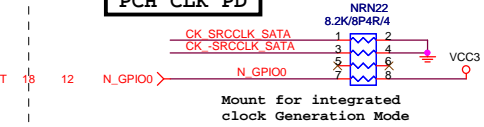
**PCH (C)**



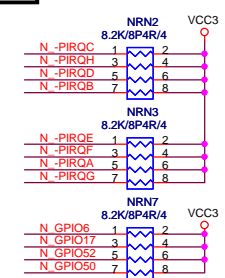
**PCH (A)**



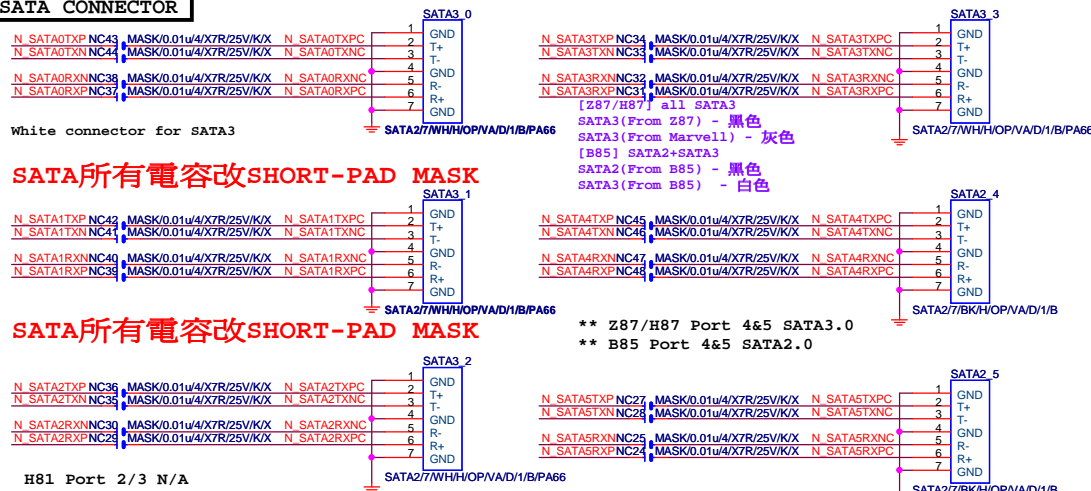
PCH	CLK	PD
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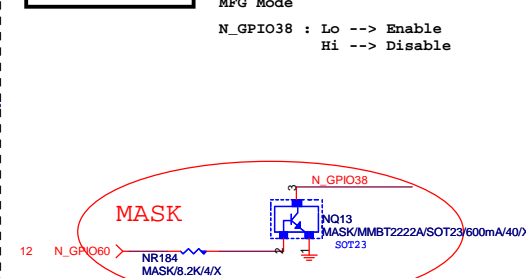
PCH	PU/PD
-----	-------



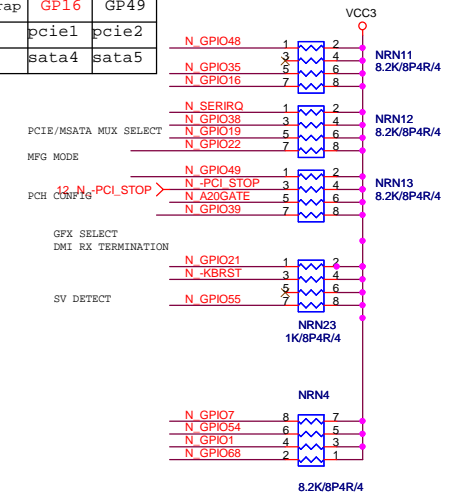
## SATA CONNECTOR



GPIO38 Ctrl



	soft strap	GP16	GP49
0		pcie1	pcie2
1		sata4	sata5

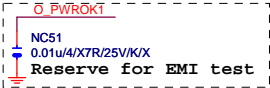
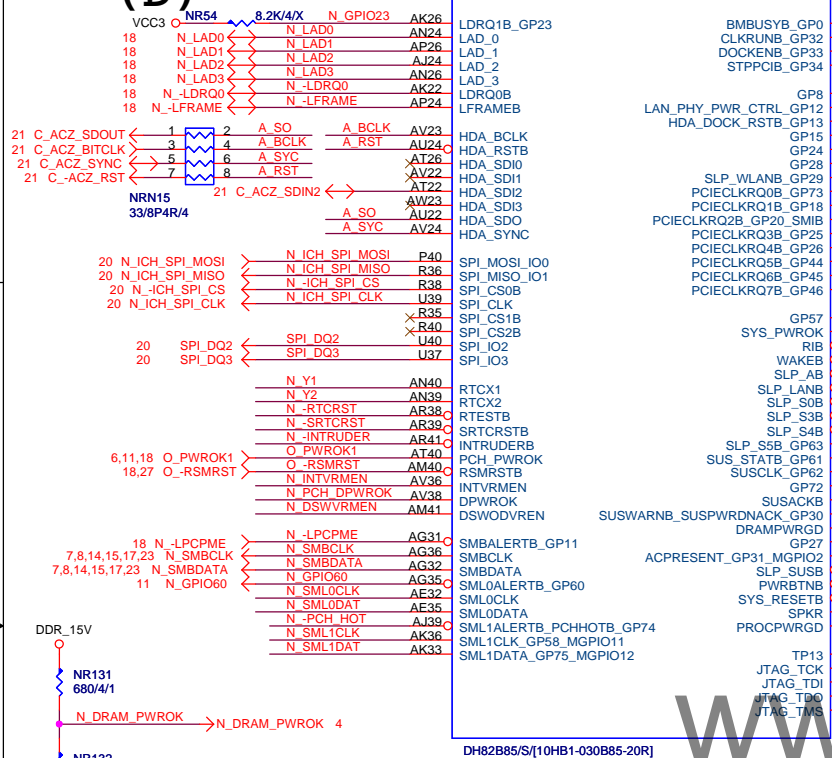


## Gigabyte Technology

Title			
PCH HOST , SATA, PCI			
Size	Document Number	Rev	
Custom	GA-B85-D3V-SI	2.01	
Date:	Thursday, November 20, 2014	Sheet	11 of 34

# PCH

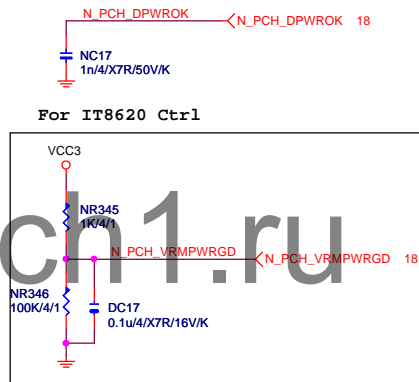
(D)



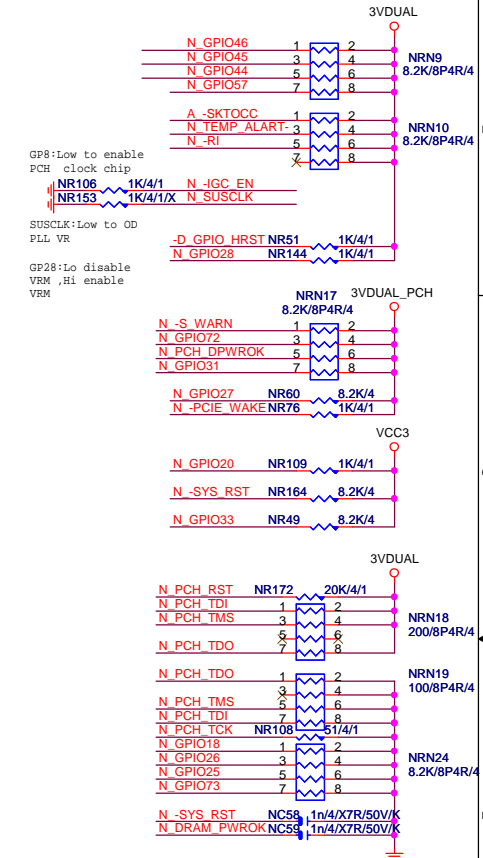
# ACZ\_SDOUT

C\_ACZ\_SDOUT : HI --> ME Enable  
Lo --> ME Disable  
HI:disable ME and override SPI Flash Access Permissions

# PCH\_DPWROK

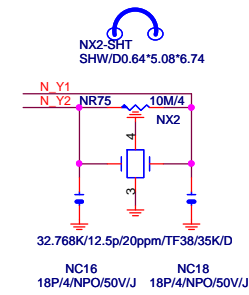


# PCH PU/PD

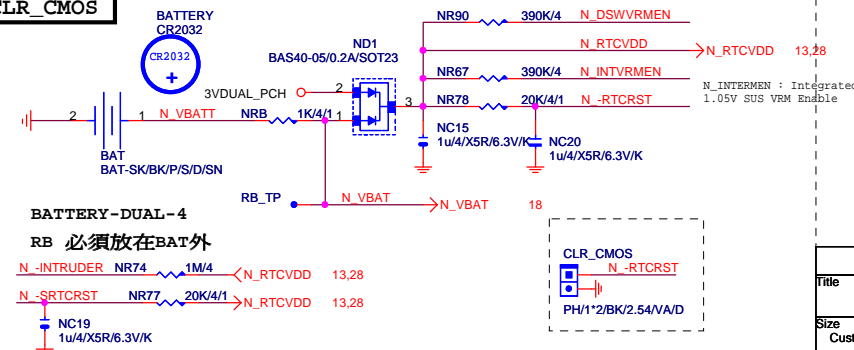


# HSW\_STRAP13

# 32.768KHZ



# CLR\_CMOS



# Gigabyte Technology

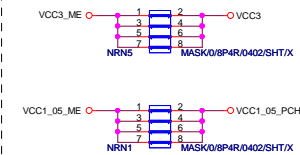
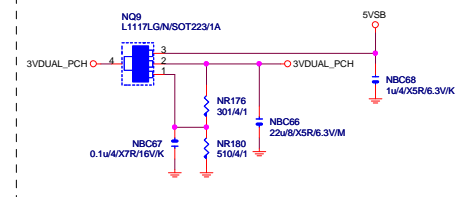
# PCH GPIO , CTRL , AUDIO

Size	Document Number	Rev
Custom	GA-B85-D3V-SI	2.01
Date:	Thursday, November 20, 2014	Sheet 12 of 34

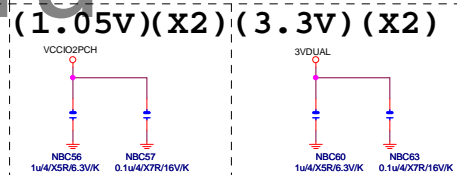
**PCH (I)**



SHT PWR

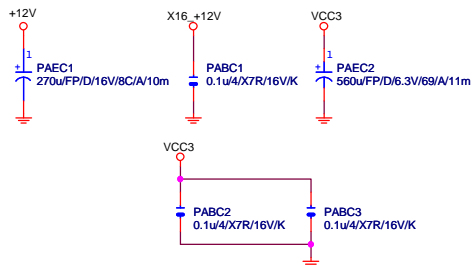


(1.05V) (x5)



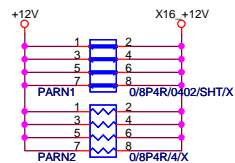


## PCIEX16 CAP



## PCIEX16 PROTECT SHT

```
+12 protect
short-wire test
```



PCIEX16	AC	CAP
---------	----	-----

PA EXP TXP0	PAC5	0.22u4/XSR/6.3VK	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/XSR/6.3VK	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/XSR/6.3VK	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/XSR/6.3VK	PA EXP TXN1 C
PA EXP TXP2	PAC5	0.22u4/XSR/6.3VK	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/XSR/6.3VK	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/XSR/6.3VK	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/XSR/6.3VK	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/XSR/6.3VK	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/XSR/6.3VK	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/XSR/6.3VK	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/XSR/6.3VK	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/XSR/6.3VK	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/XSR/6.3VK	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u4/XSR/6.3VK	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u4/XSR/6.3VK	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/XSR/6.3VK	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/XSR/6.3VK	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/XSR/6.3VK	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/XSR/6.3VK	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/XSR/6.3VK	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/XSR/6.3VK	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/XSR/6.3VK	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/XSR/6.3VK	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/XSR/6.3VK	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/XSR/6.3VK	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/XSR/6.3VK	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/XSR/6.3VK	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/XSR/6.3VK	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/XSR/6.3VK	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/XSR/6.3VK	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/XSR/6.3VK	PA EXP TXN15 C

PCI-E REV:1.1--&gt; 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz\*(8b/10b)=2Gb/s=250MB/s

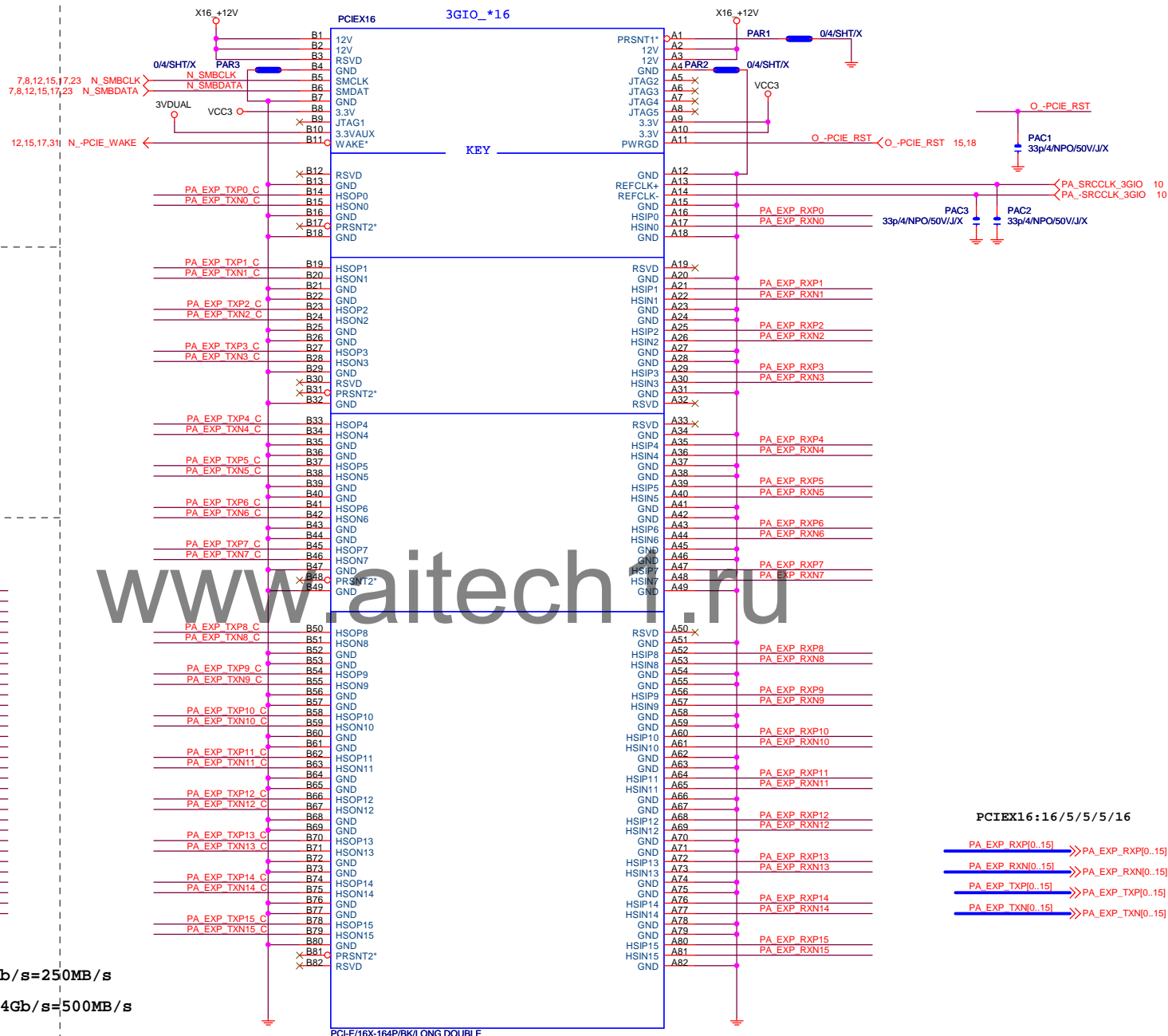
PCE-E X1(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz\*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz\*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--&gt; 5GHZ

## PCIEX16 SLOT



PCI-E/16X-164P/BK/1 ONG DOUBI E

PCIEX16:16/5/5/5/16

PA\_EXP\_RXP[0..15] \\ PA\_EXP\_RXP[0..15]\_4

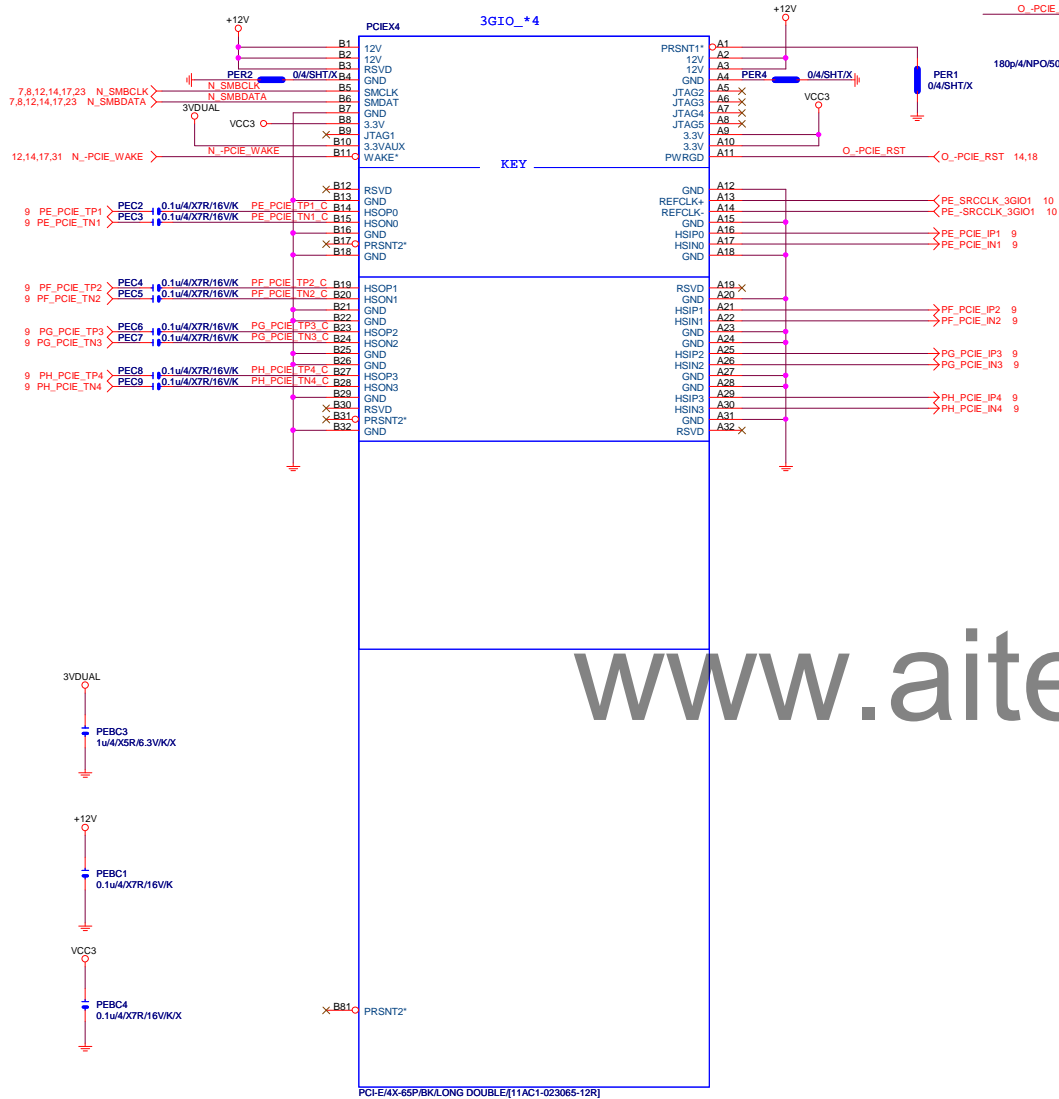
PA\_EXP\_RXN[0..15] >> PA\_EXP\_RXN[0..15] 4

PA\_EXP\_TXP[0..15]  $\gg$  PA\_EXP\_TXP[0..15] 4

PA\_EXP\_TXN[0..15] >> PA\_EXP\_TXN[0..15] 4

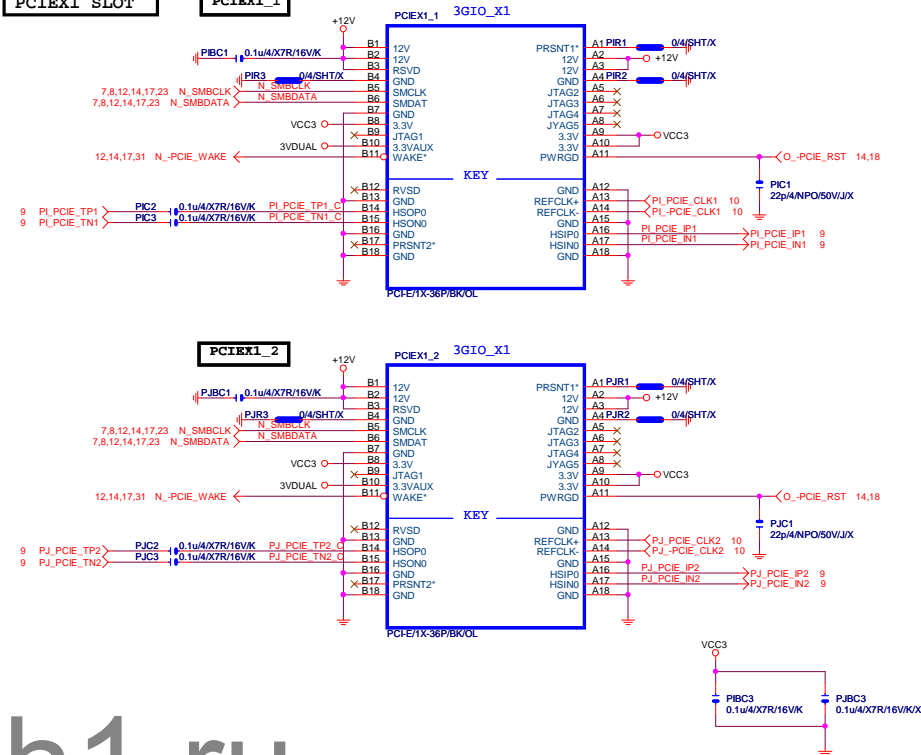
<b>Gigabyte Technology</b>			
Title <b>PCI EXPRESS * 16</b>			
Size Custom	Document Number	<b>GA-B85-D3V-SI</b>	Rev <b>2.0</b>
Date:	Thursday, November 20, 2014	Sheet	14 of 34

PCIEX4 SLOT
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## PCIEX1 SLOT

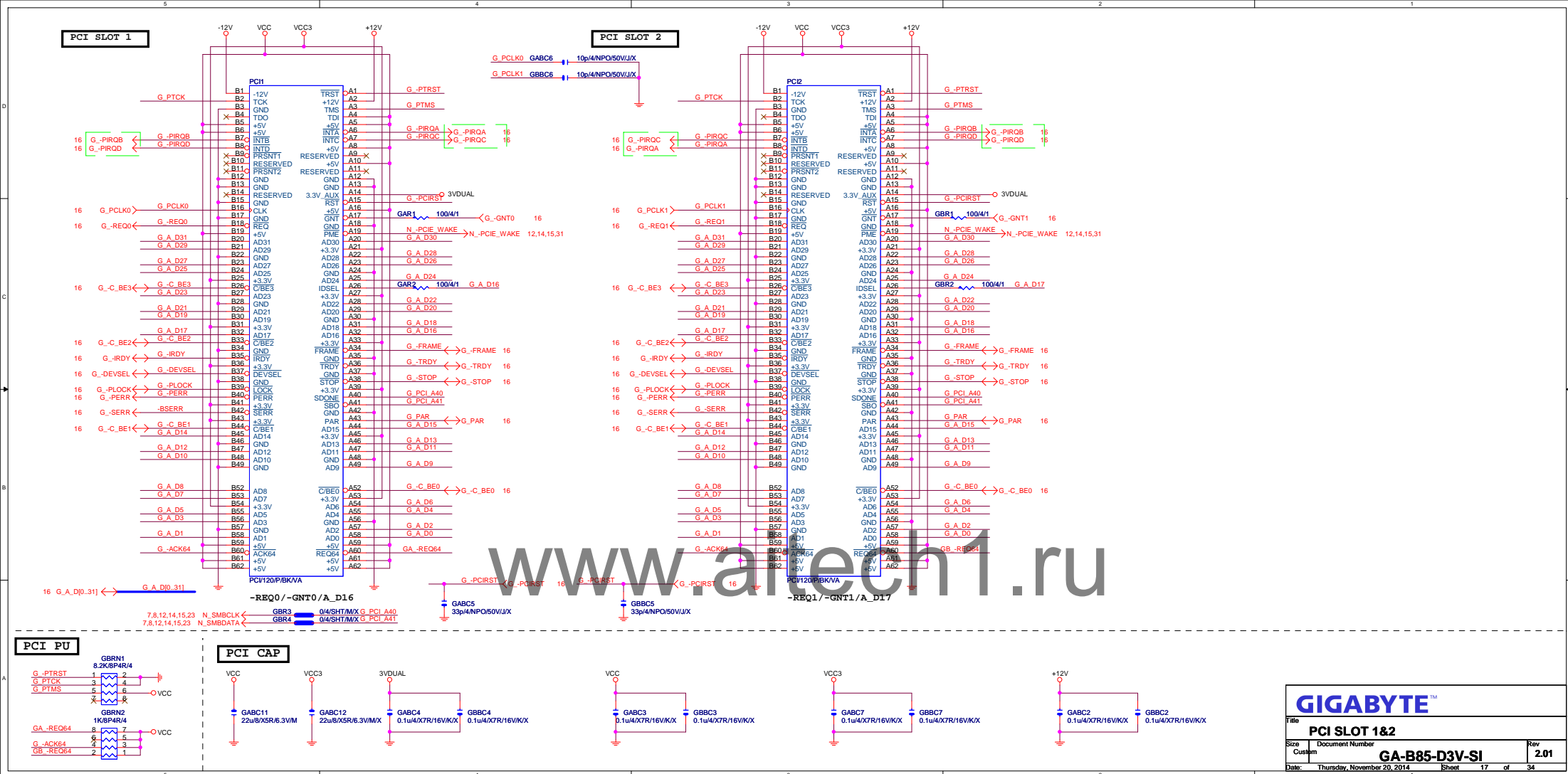
## PCIEX1\_1



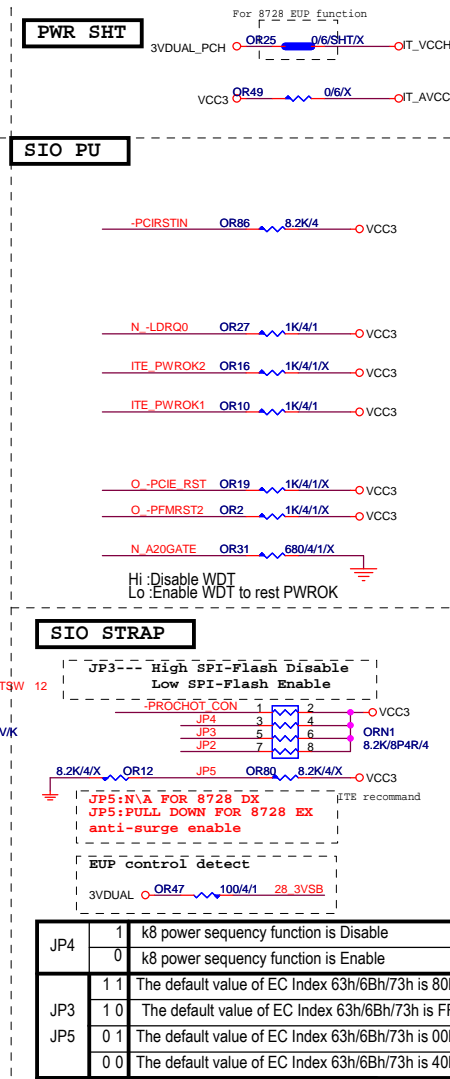
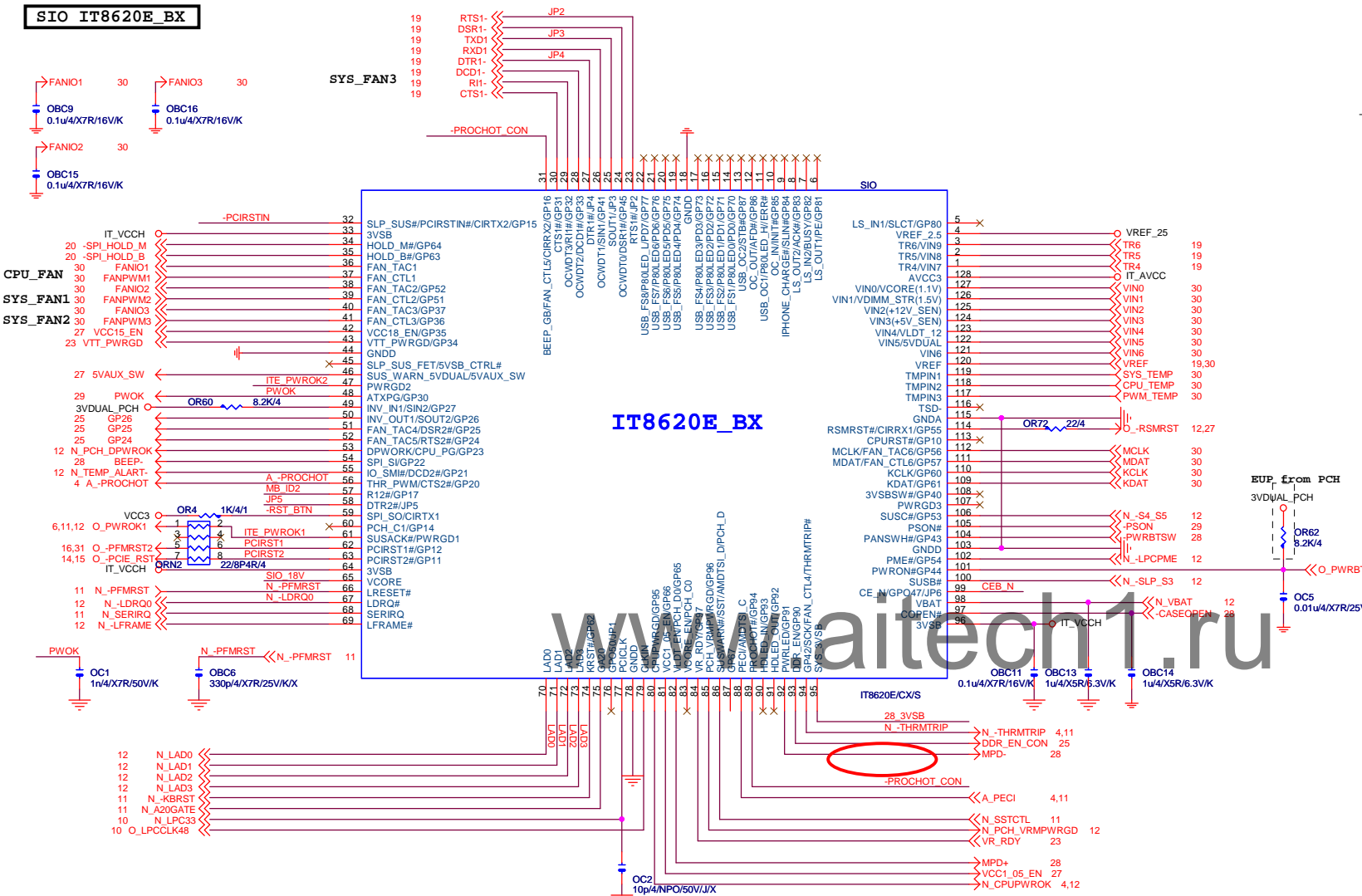
www.aitech1.ru





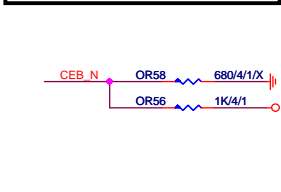


# SIO IT8620E\_BX

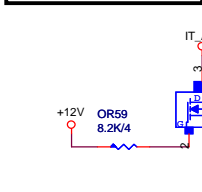


IT8620E GPIO問題調整	
PIN 50	第一次接上POWER時會拉 LO
PIN 90/91	DEFAULT為HIDLED FUNCTION, GP93 BYPASS TO GP92
PIN 108	GP40---- POWER ON 時會拉 LO
PIN 111/112	MOUSE 跟PAN6 FUNCTION 擇一使用,不然會互相干擾

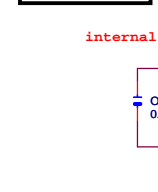
## DUAL BIOS OPT STRAP



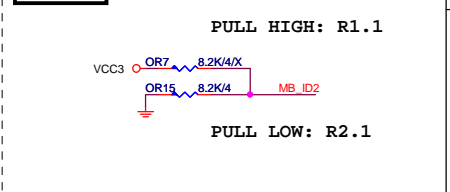
## Power leakage



## SIO\_18V



## MB ID

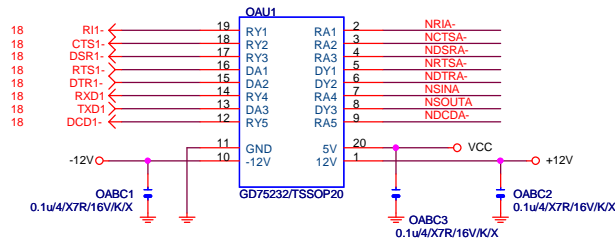


## SIO CAP

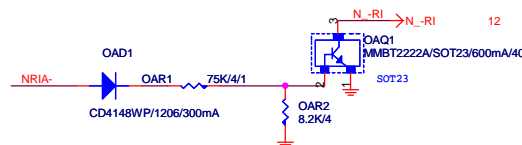


Gigabyte Technology			
Title	ITE 8728 LPC IO		
Size	Document Number	GA-B85-D3V-SI	
Custom		Rev 2.01	
Date:	Thursday, November 20, 2014	Sheet	18 of 34

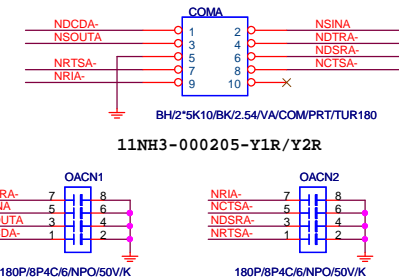
## COMA



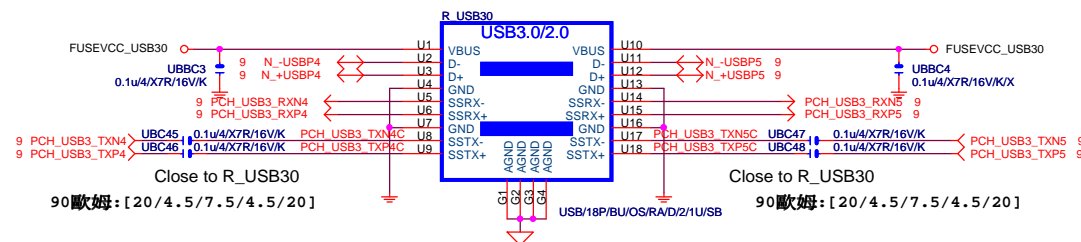
## COM RI



## COM BUFFER

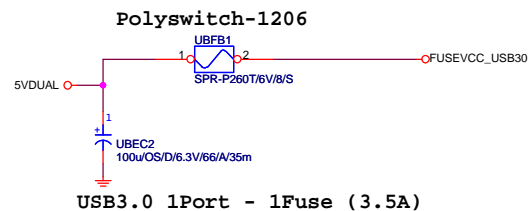


## USB30\_20 CONNECT

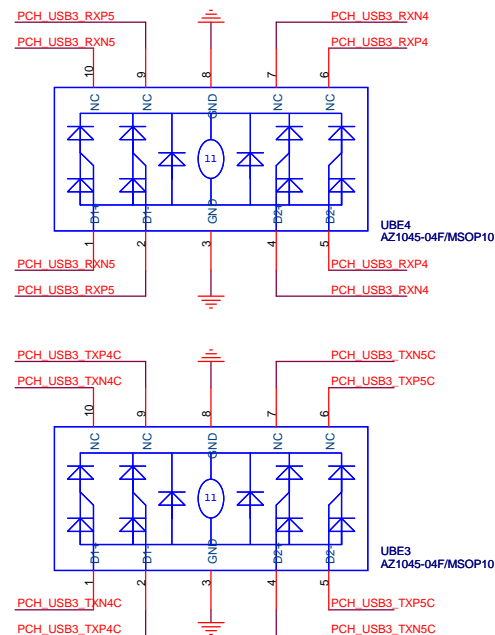


## -PROHOT

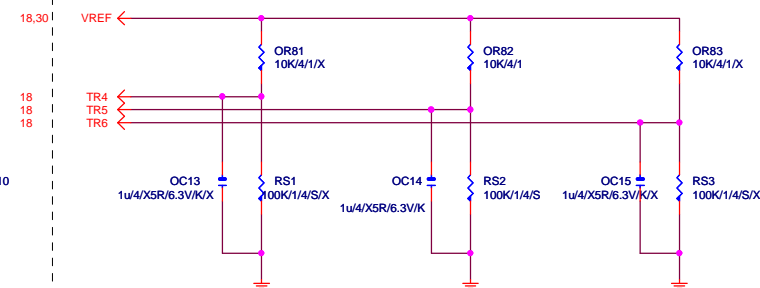
## USB30 PWR



## USB30 ESD PROTECT

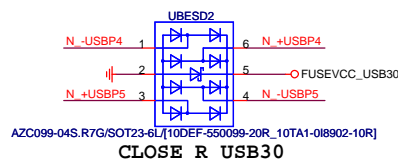


## -PROHOT



RS1 close DBQ1、  
RS2 close DDQ1、  
RS3 close DAQ1、  
Others close SIO

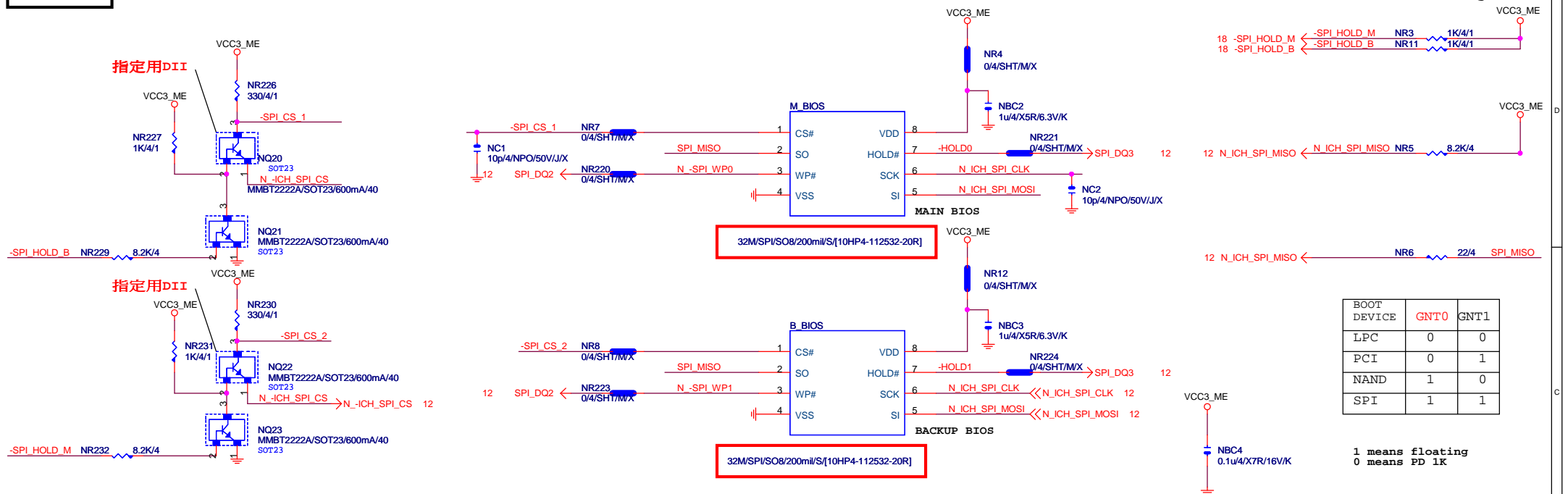
## USB20 ESD PROTECT



Gigabyte Technology

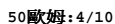
COM & PROHOT/Dynamic O.C.			
File	Document Number	GA-B85-D3V-SI	Rev 2.01
Size	Custom		
Date:	Thursday, November 20, 2014	Sheet	19 of 34

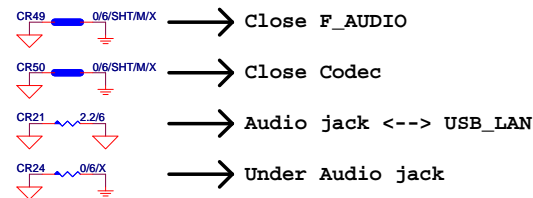
**DUAL BIOS**



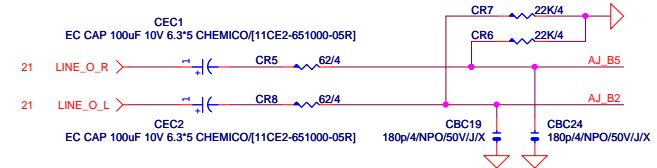
www.aitech1.ru

CR14/CBC4 close to PCH





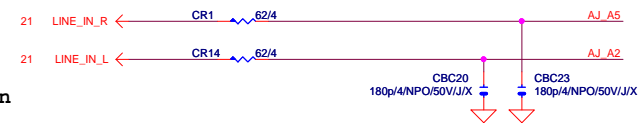
## LINE-OUT



## LINE-IN

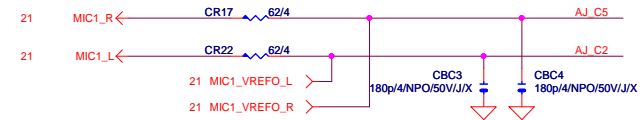
Verify MIC function  
 in LINE-in

Only reserved for ALC888



For 889A/888

## MIC-IN

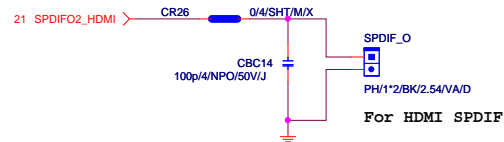


## SURROUND

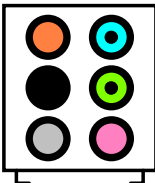
## CEN/LFE

## SURR BACK

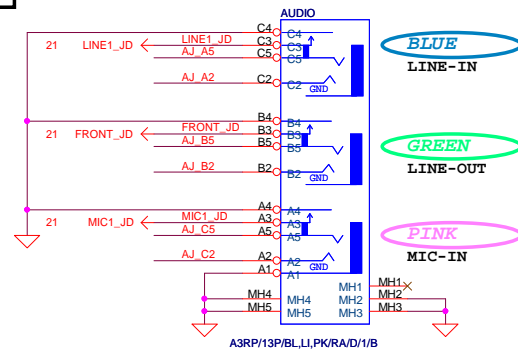
## SPDIF\_OUT



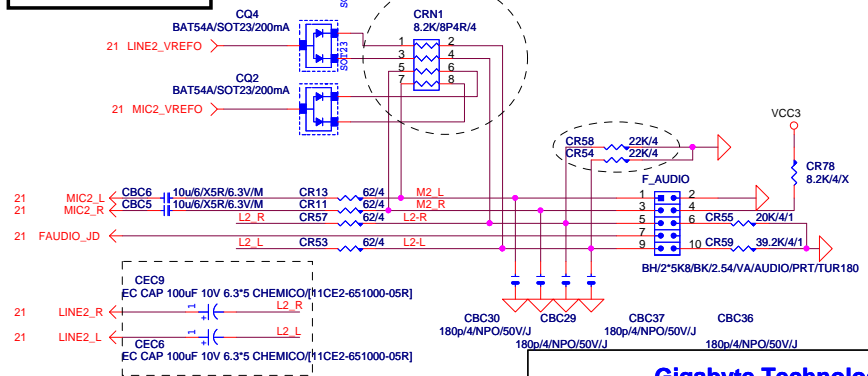
## AZALIA JACK



## AZALIA JACK



## AZALIA FRONT PANEL

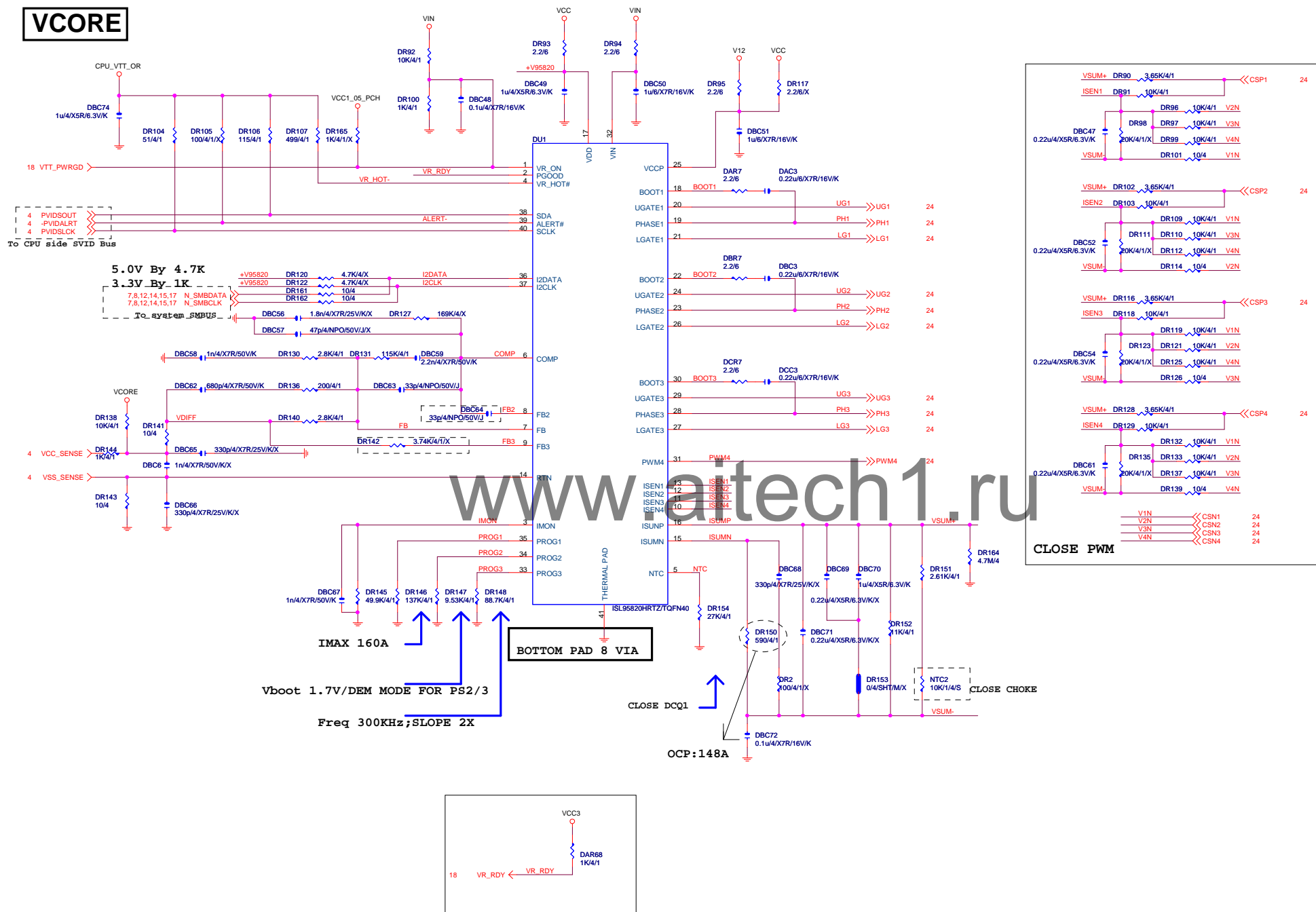


Gigabyte Technology

Title		
AUDIO JACK		
Size Custom	Document Number	Rev
	GA-B85-D3V-SI	2.01
Date:	Thursday, November 20, 2014	Sheet 22 of 34

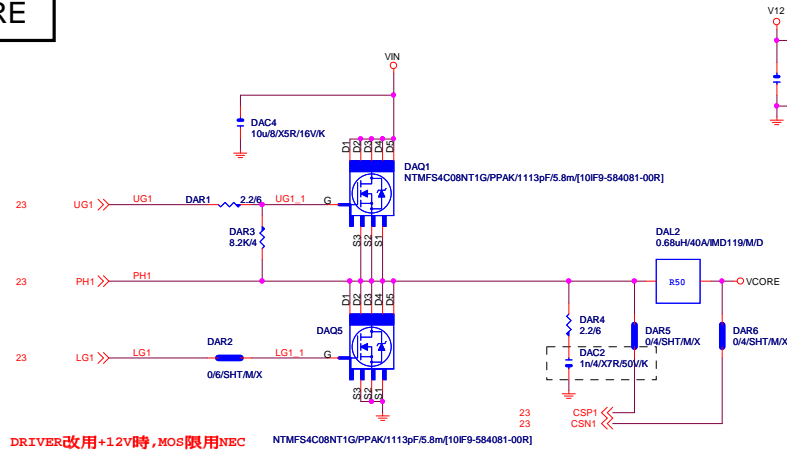
www.aitech1.ru



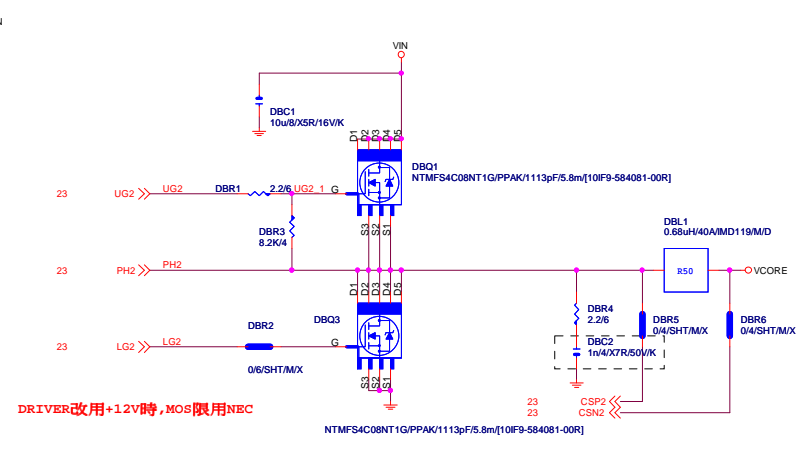
**VCORE**

# VCORE

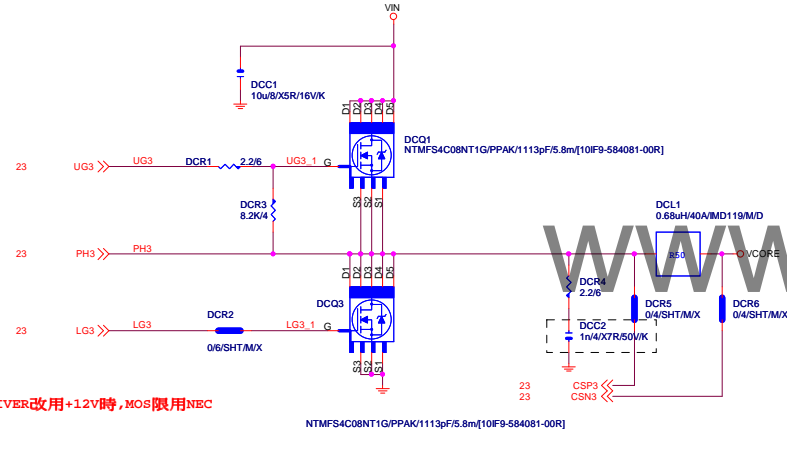
[ 1 ]



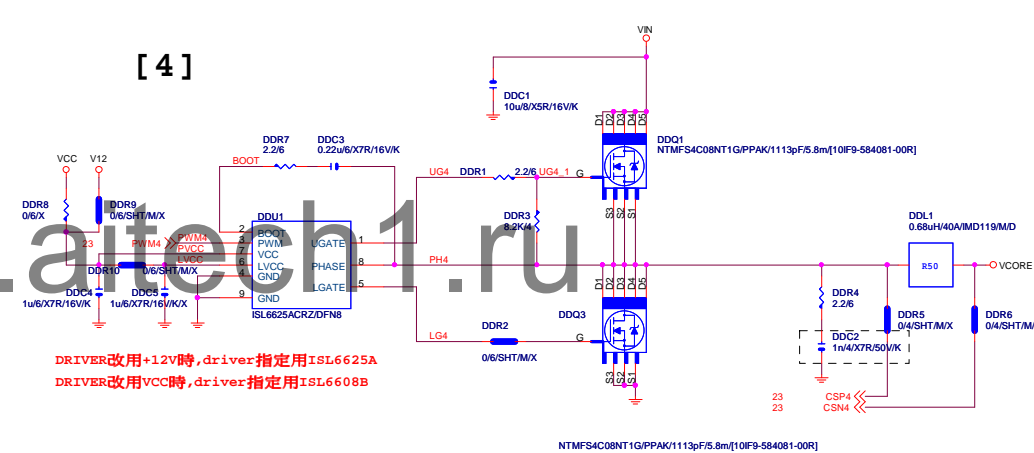
[ 2 ]



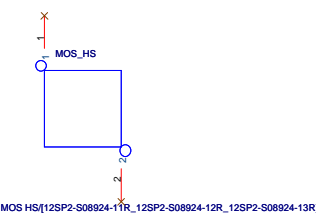
[ 3 ]



[ 4 ]



# MOSFET HEATSINK

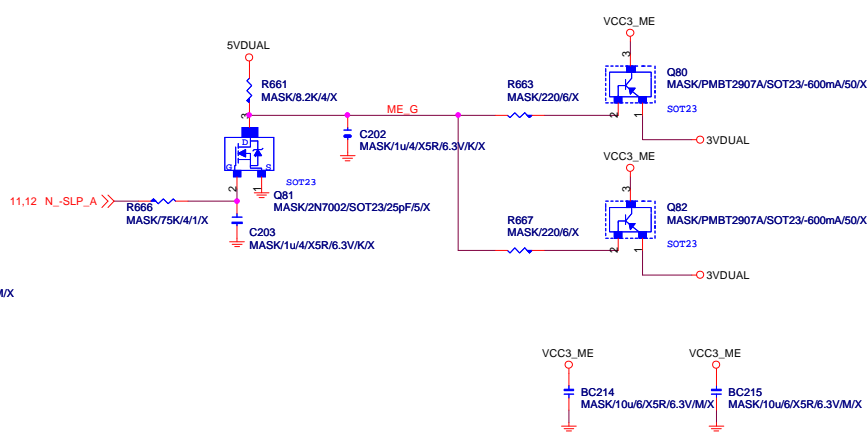
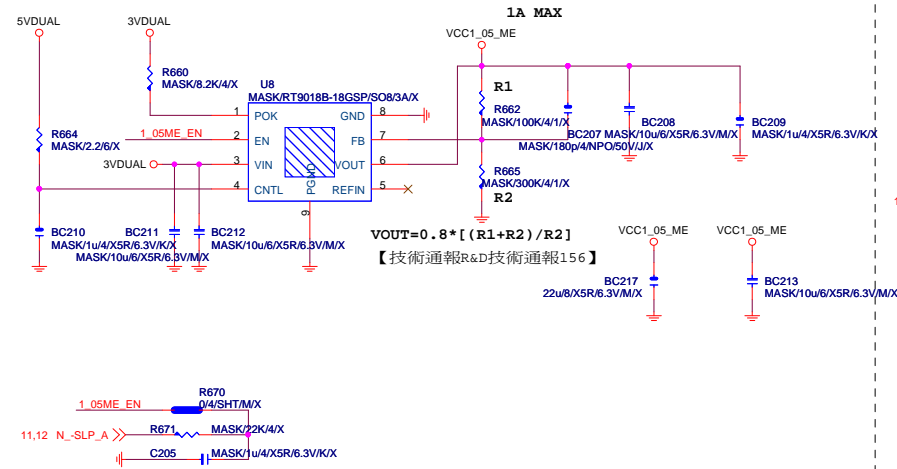


Gigabyte Technology			
Title	ISL95820_2		
Size	Document Number	GA-B85-D3V-SI	
Custom			Rev 2.01
Date	Thursday, November 20, 2014	Sheet 24	of 34

## VCC1\_05\_ME

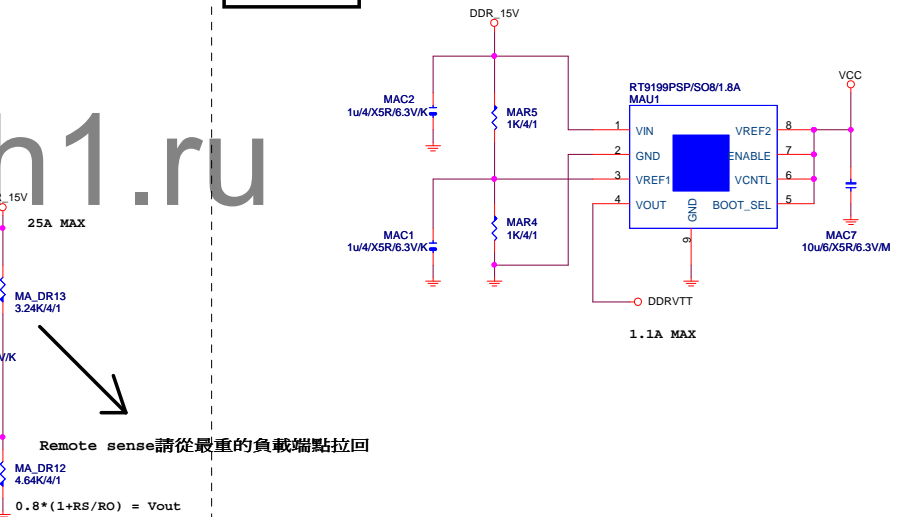
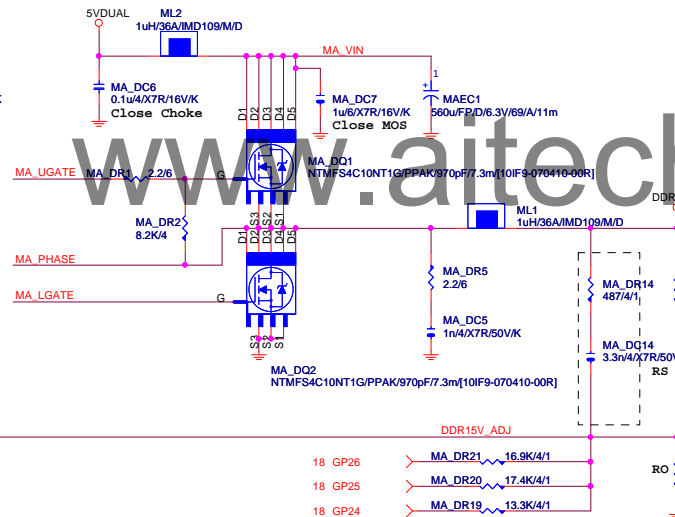
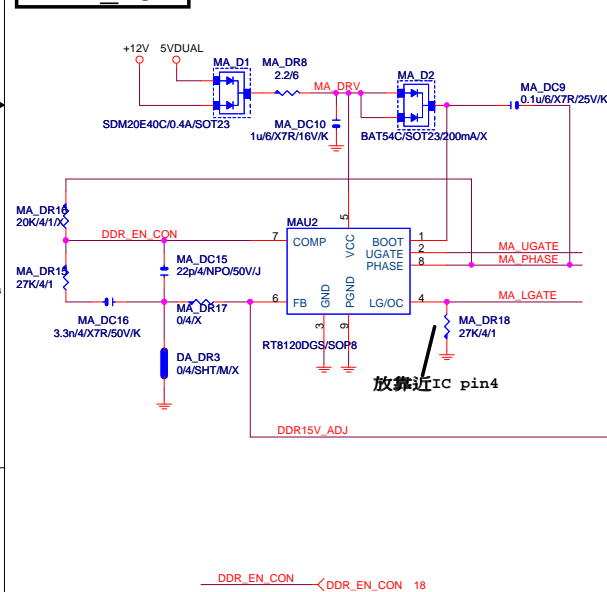
【技術通報R&D技術通報156】  
(RICHTEK), (NUVOTON), (EMC)做共用  
PIN7分壓阻值須修改為100K以上電阻值

## VCC3\_ME



## DDR\_15V

## DDRVTT



VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1  
IRMS=11.45A  
560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A  
Coefficient=1.7(85°C), 1(105°C)  
VIN Ripple current=4.7X1.7=7.99A(85°C)  
-->故固態電容須2x7.99=15.98>11.45A  
OCP:25A for Rds=8.9~10.8m for on@4.5V  
OCP:25A for Rds=5.8~6.95m for on@10V  
OCP:46.55~25A=Roset\*Iocset / Rds(on)  
=27K\*10uA / 5.8~10.8

GIGABYTE™			
Title			
DDR15V / M3 POWER			
Size	Document Number	Rev	
Custom	GA-B85-D3V-SI	2.01	
Date:	Thursday, November 20, 2014	Sheet	25 of 34

OVER VOLTAGE

NCT3933	0X2A	0X20	0X22
VREF1	DDRVTT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

## Gigabyte Technology

Title

## CPU CORE VR-2

Size  
Custom

Document Number
-----------------

GA-B85-D3V-SI

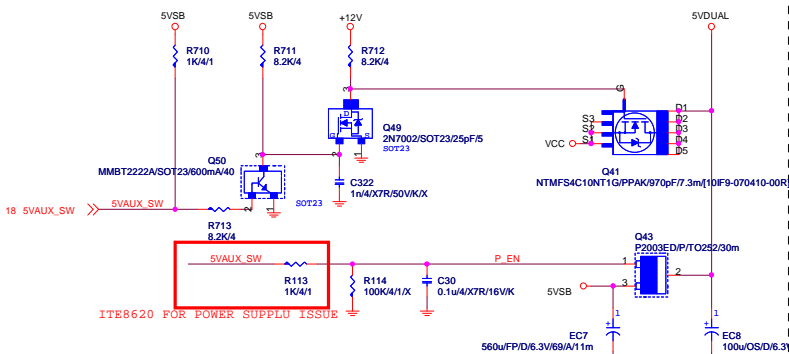
Rev	2.01
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Date:

Date: Thursday, November 20, 2014 Sheet 26 of 34

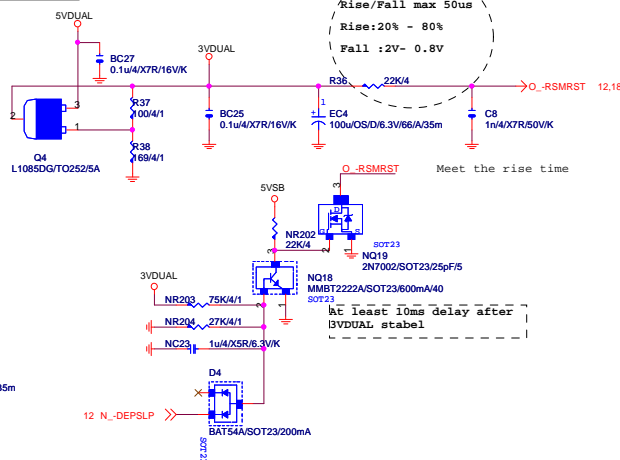
2	1
---	---

## 5VDUAL

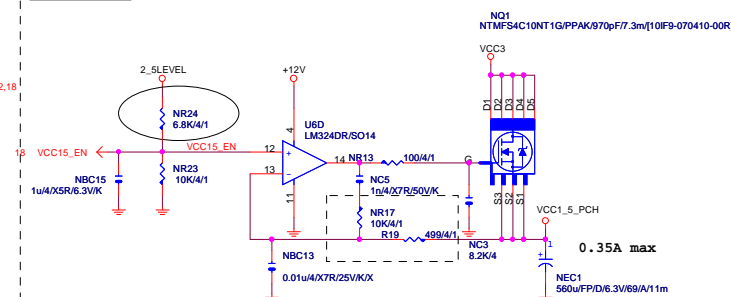


5VSB OVP發生時 : 5VDUAL=0.8V --> 解除時,須拔POWER CORE 才可開機

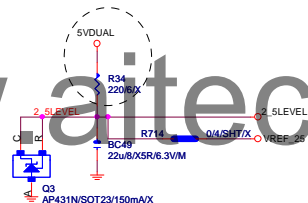
## 3VDUAL



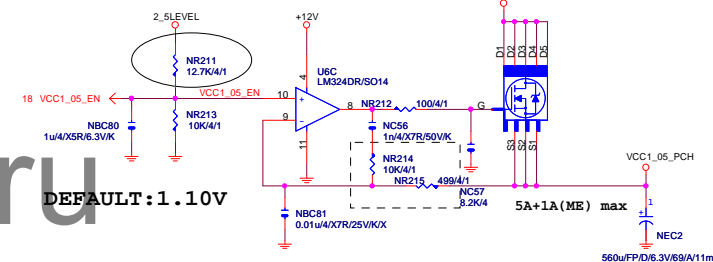
## VCC1\_5\_PCH



ERP



## VCC1 05 PCH

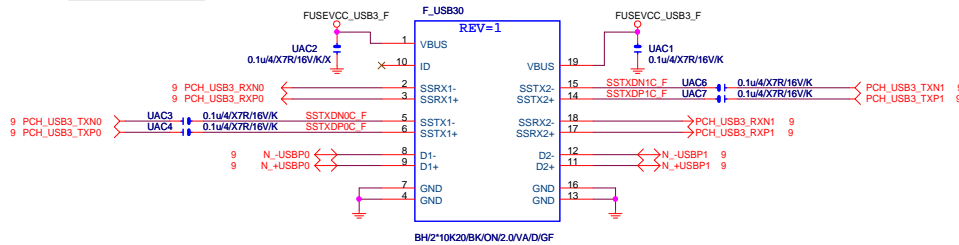


DEFAULT:1.10V

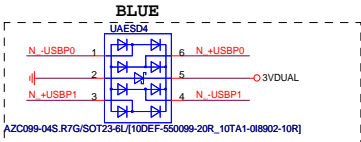
## Gigabyte Technology

Title			
<b>DISCRETE POWER</b>			
Size	Document Number		Rev
Custom	<b>GA-B85-D3V-SI</b>		<b>2.01</b>
Date:	Thursday, November 20, 2014	Sheet	27 of 34

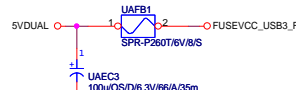
# Front USB3.0



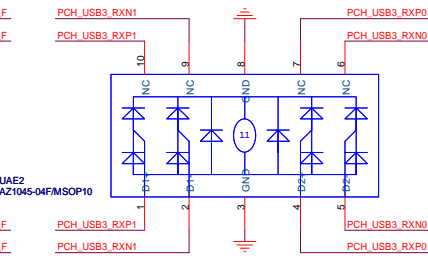
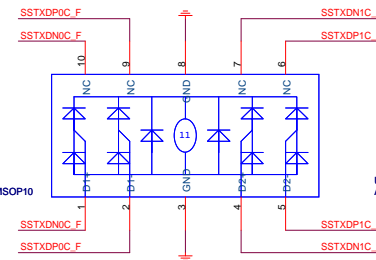
# F\_USB30 PWR



Close to connector

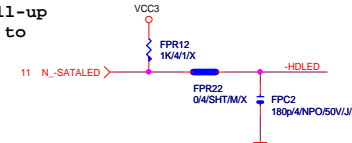


# F\_USB30 ESD PROTECT

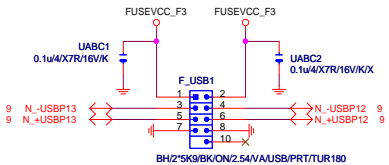


# SATA LED

SATALED# signal open-collector,pull-up (8.2 kΩ to 10 kΩ) to Vcc3\_3

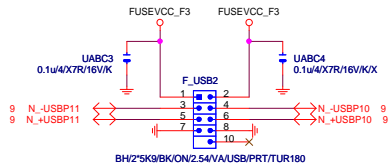


# FRONT USB1



Close to connector

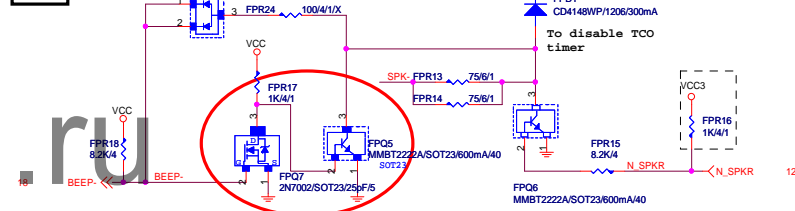
# FRONT USB2



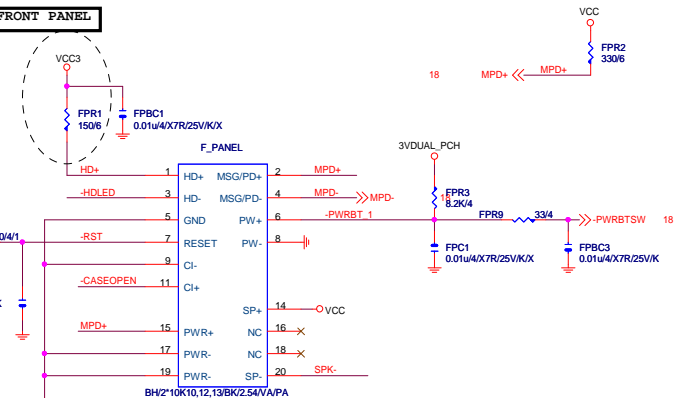
Close to connector

USB2.0 Signal & power short protection  
USB2.0 Signal set 4.8V (If bigger than 4.95V, chip maybe fail)  
Protection set --> 3VUUAL=3.6V

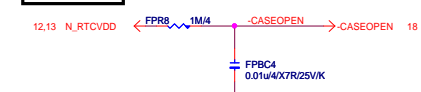
# SPKR



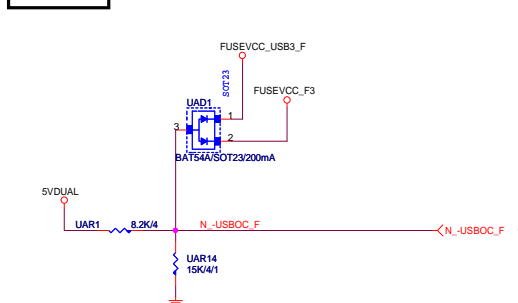
# INTEL FRONT PANEL



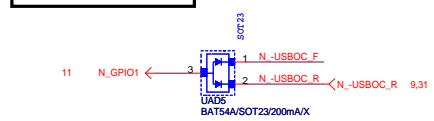
# CASE OPEN



# -USBOC\_F



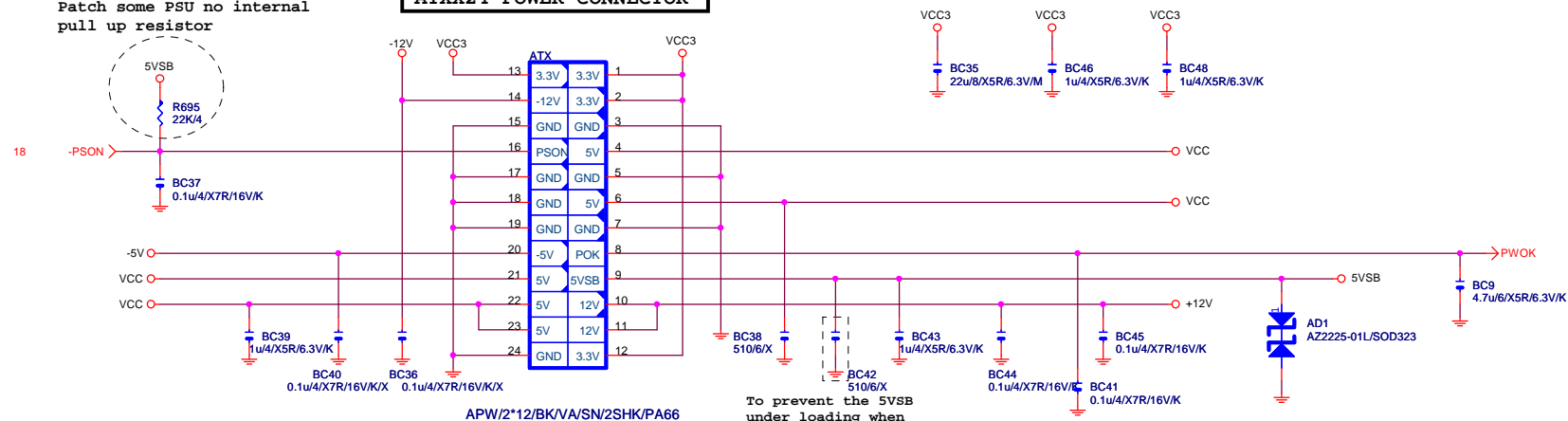
# F\_USB POWER PROTECT



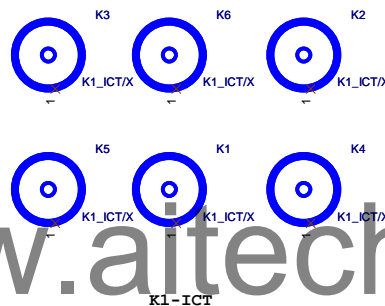
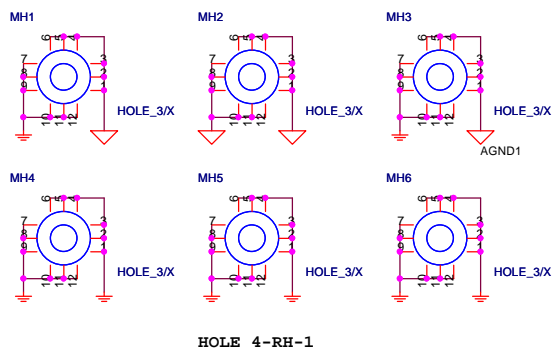
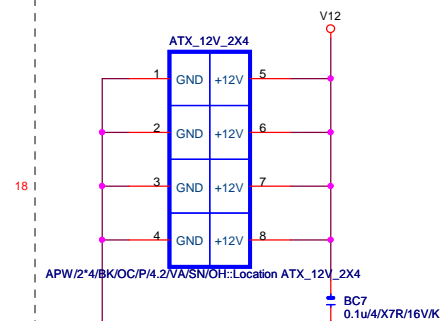
Gigabyte Technology			
Title		FP,F_USB,USB PWR,FDD,BZ	
Size		Document Number	
Custom		GA-B85-D3V-SI	
Date:		Thursday, November 20, 2014	
Sheet		28 of 34	

Patch some PSU no internal pull up resistor

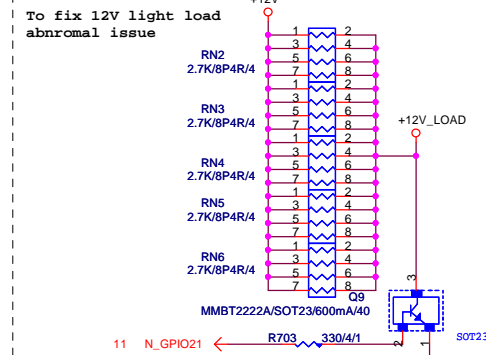
# ATXX24 POWER CONNECTOR



# ATXX4 POWER CONNECTOR

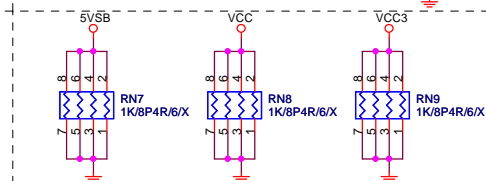


# 【技術通報R&D技術通報153】



# PWOK PATCH

# 【技術通報R&D技術通報154】



Gigabyte Technology

Title		
ATX POWER CONNECTOR		
Size	Document Number	Rev
Custom	GA-B85-D3V-SI	2.01
Date:	Thursday, November 20, 2014	Sheet 29 of 34



TEMP H/W MONITOR

VREF

OR73 10K/4/1

R674 8.2K/4

R675 8.2K/4

SYS\_TEMP

CPU\_TEMP

PWM\_TEMP

OC7 1u4/XSR/6.3V/K

OC8 1u4/XSR/6.3V/K

RS\_SYS 10K/1/4/S

Close SIO

Close to SIO

The schematic diagram illustrates the CPU\_FAN circuit. It features a +12V supply connected to a 3.3K/4/1 resistor (R673). The output of R673 is connected to a 15K/4/1 resistor (R677), which is then connected to a 6.2K/4/1 resistor (R678). The output of R678 is connected to the FANIO1 pin (18) of the CPU SMART FAN module. A 0.1u4/X7R/16V/K capacitor (C233) is connected between the +12V supply and ground. A 1u6/X7R/16V/K capacitor (C233) is connected between the output of R677 and ground. A BC64 diode is connected between the output of R677 and the output of R678. The CPU\_FAN (FAN1\*4/WH/A3/PA66) is connected to the output of R678. The CPU SMART FAN module is labeled with various components and their values.

**VOLTAGE-- H/W MONITOR**

Trt728 bX  
\*\* IT8728 CX

VIN2 must +12V input  
VIN3 must VCC input

Close to SIO

The division voltage of VIN2 & VIN3 must be around 2.9V

**KB/USB**

18 KDAT <-> R2 82/6 KBDATA  
 18 KCLK <-> R3 82/6 KBCLK  
 18 MDAT <-> R4 82/6 MSDATA  
 18 MCLK <-> R5 82/6 MCLK

18p8B4C/6/NPO/50V/K

CN1

18p8B4C/6/NPO/50V/K

AGND1

FUSEVCC\_R1

FUSEVCC\_R1

BC2 0.1u/4X7R/16V/K

9 N\_-USBP8 <-> U6  
 9 N\_+USBP8 <-> U7

U5  
 U6  
 U7  
 U8

KB MS USB

U5B

1 KBDATA  
 2 MSDATA  
 5 KBCLK  
 6 MCLK

AGND1

4 AGND1

FUSEVCC\_R1

9 N\_-USBP9  
 9 N\_+USBP9

U2  
 U3  
 U4

KB

3 AGND1

KB/USB/A/PC99(DUAL)/GF/2/RAID

AGND1

FUSEVCC\_R1

RN1 8.2K/8P4R/6

1 2 MCLK  
 3 4 MDAT  
 5 6 KCLK  
 7 8 KDAT

E5D2

1 N\_-USBP8  
 2  
 3 N\_+USBP9

6 N\_+USBP8  
 5 FUSEVCC\_R1  
 4 N\_-USBP9

AZC099-04S.R7/G/SOT23-6L(10DEF-550099-20R\_10TA1-018902|10R)

5VDUAL

UBF8 SPR-P200T/6V/8/S

FUSEVCC\_R1

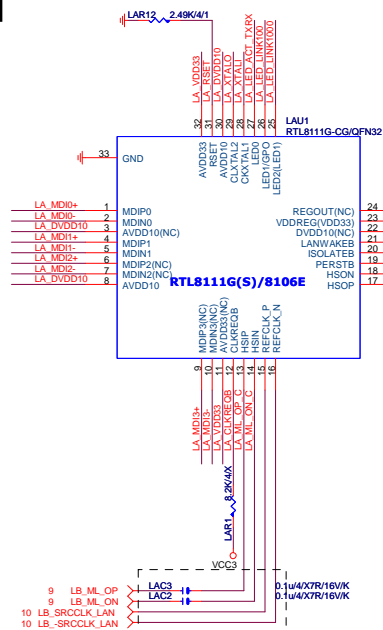
UBEC1 100u/OS/D.6.3V/66/A/35m

[illegible]

The schematic diagram illustrates the SYS\_FAN2 circuit. It features a fan controller IC (U15, NCT3941S-A/SOP8-EP) which is connected to a fan (SYS\_FAN2, FAN114BK/A3/PA66). The circuit is powered by a +12V supply. Key components include resistors R681 (1K/4/1), R684 (2K/4/1), R683 (8.2K/4/1), R118 (3.3K/4/1), and R120 (6.2K/4/1). Capacitors FC2 (1u6/X7R/16V/K) and FC5 (10u6/X5R/16V/K) are used for timing and filtering. A BC218 transistor is connected to the fan's VOUT signal. The fan's VOUT signal is also connected to FANIO3. The schematic is labeled with component values and pin numbers.

[illegible]

# LAN



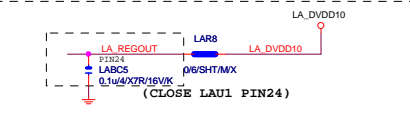
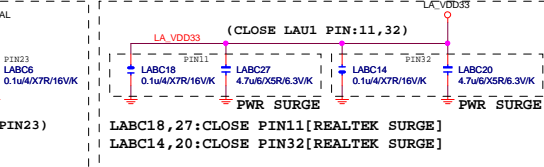
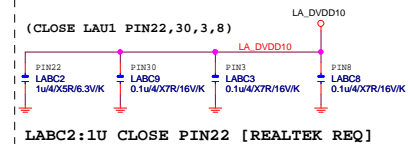
SRCCLK-->50歐姆:[18/4/10/4/18]

LA\_ML-->80歐姆:[15/5/5/5/15]

離IC近越好

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# LAN POWER



NOTE:  
RT8106E:PIN3,11,22,24-->NC  
LABC2LABC3,LABC5,LABC18,LABC27-->N/A

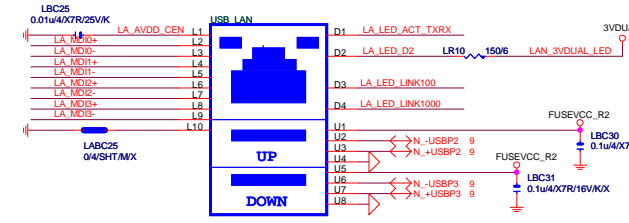
料號	規格	廠商
11NR6-702009-96R	1G LAN (12core)	UDE(RU9 ESD+)
[LED獨立走線,可省略外加AZC099零件LAESD1]		

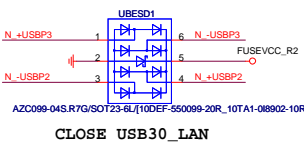
1.	9KV ESD BOM:
	USB_LAN (RU9):11NR6-702009-96R
2.	28KV ESD BOM:
	USB_LAN (RU9):11NR6-702009-96R
	LAESD2,LAESD1,LAESD3

# USB30\_LAN CONNECTOR

100歐姆:[20/4/10/4/20]

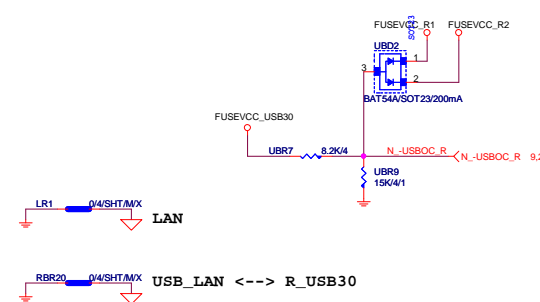


90歐姆:[12/5/7/5/12]



CLOSE USB30\_LAN

# -USBOC\_R



Gigabyte Technology			
File	Realtek RTL8111G		
Size	Document Number	GA-B85-D3V-SI	
Custom		Rev	2.0
Date:	Tuesday, November 25, 2014	Sheet	31 of 34

DVI NON LEVEL SHIFT

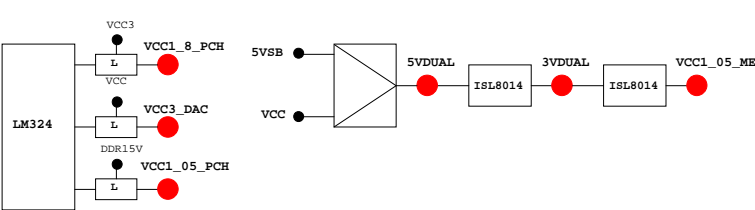


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Gigabyte Technology		
Title		
VL805 USB3.0		
Size	Document Number	Rev
Custom	GA-B85-D3V-SI	2.01
Date:	Thursday, November 20, 2014	Sheet 33 of 34

PIN NAME	PWR	AFTER PLUGST	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI	GPIO0	N/A
GP1/TACH1	MAIN		GPI	GPIO1	N/A
GP2/PIRQE#	MAIN		GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN		GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN		GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN		GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN		GPI	PCIEX1 Detect	P/U 8.2K VCC3
GP7/TACH3	MAIN		GPI	GPIO7	P/U 8.2K VCC3
GP8	STBY	H	GPI	GPIO8	N/A
GP9/OC5#	STBY		NATIVE	USB OC5#	N/A
GP10/OC6#	STBY		NATIVE	USB OC6#	N/A
GP11/SMBALERT#	STBY		NATIVE	USB PWR protect	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI	GPIO12	N/A
GP13	STBY	L	GPI	LPCPME#	P/U 8.2K 3VDUAL
GP14/OC7#	STBY		NATIVE	USB OC7#	N/A
GP15	STBY	L	GPI	GPIO15(TL8 Enable)	P/U 8.2K 3VDUAL
GP16	MAIN		GPI	GPIO16	P/U 8.2K VCC3
GP17/TACH0	MAIN		GPI	GPIO17	P/U 8.2K VCC3
GP18	MAIN		GPI	Mobile Only	N/A
GP19	MAIN		GPI	GPIO19	P/U 8.2K VCC3
GP20	MAIN		GPI	GPIO20	P/U 8.2K VCC3
GP21	MAIN		GPI	GPIO21	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI	GPIO22	P/U 8.2K VCC3
GP23	MAIN		GPI	GPIO23	N/A
GP24	STBY	L	GPI	SKTOCC#	N/A
GP25	STBY			Mobile Only	N/A
GP26	STBY			Mobile Only	N/A
GP27	STBY	H	GPO	GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO	FWR LED	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI	GPIO29	N/A
GP30	STBY	H-Z	GPI	Mobile Only	N/A
GP31	STBY	H-Z	GPI	Mobile Only	N/A
GP32	MAIN	H	GPO	N/A	N/A
GP33	MAIN	H	GPO	N/A	N/A
GP34	MAIN	H-Z	GPI	-PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO	-ACZ_DET	P/U 8.2K VCC3
GP36	MAIN		GPI	N/A	N/A
GP37	MAIN		GPI	N/A	N/A
GP38	MAIN	H-Z	GPI	PCIEX4 Detect	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI	GPIO39	P/U 8.2K VCC3
GP40	STBY		NATIVE	USB OC1#	N/A
GP41	STBY		NATIVE	USB OC2#	N/A
GP42	STBY		NATIVE	USB OC3#	N/A
GP43	STBY		NATIVE	USB OC4#	N/A
GP44	STBY	L	NATIVE	GPIO44	P/U 8.2K 3VDUAL
GP45	STBY		NATIVE	GPIO45	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE	GPIO46	P/U 8.2K 3VDUAL
GP47	STBY			Mobile Only	N/A
GP48	MAIN	H-Z	IN	GPIO48	P/U 8.2K 3VDUAL
GP49	MAIN	H-Z	IN	GPIO49	P/U 8.2K 3VDUAL
GP50	MAIN		NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE	-GNT1	N/A
GP52	MAIN		NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE	-GNT2	N/A
GP54	MAIN		NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE	-GNT3	N/A
GP56	STBY		NATIVE	Mobile Only	N/A
GP57	STBY	H-Z	IN	VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE	F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY		NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE	-SUSTAT	N/A
GP62	STBY	L	NATIVE	SUSCLK	N/A
GP63	STBY	L	NATIVE	GPIO63	N/A
GP64	MAIN	L	NATIVE	CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE	CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE	CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE	CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE	VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY			Mobile Only	N/A
GP74	STBY	H-Z	NATIVE	1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	
PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSCH/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMB_C_R	2X PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXX2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



The diagram illustrates the power distribution architecture for the CPU. It shows the CPU VTT and VCORE power planes, the CPU SOCKET, the PCH, and the P-PACK. The CPU VTT plane includes MOSFETs (TQ3, TQ4), a CHOKE (TL1), and DC/DC converters (DC\_DQ1, DC\_DQ2, DC\_DQ3, DC\_DL1, DC\_DL2). The VCORE plane includes DC/DC converters (DA\_DQ1, DA\_DQ2, DA\_DQ3, DA\_DL1, DA\_DL2) and a CHOKE (DL2). The CPU SOCKET is connected to the PCH, which is connected to the P-PACK. The P-PACK is connected to the VCORE plane.

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Termination
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

Z77-D3H :  
PCH :  
12SP2-S05511-01R/02R/03R  
MOSFET :  
12SP2-S08924-01R/02R/03R

	3 pin fan control	4 pin fan control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH